DATA SHEET

MODULETEK:AOC-QSFP10-QSFP10-OM3-aaa.aaM-C0C0C

40Gb/s QSFP+ Active Optical Cable

AOC-QSFP10-QSFP10-OM3-aaa.aaM-C0C0C Overview

ModuleTek’s AOC-QSFP10-QSFP10-OM3-aaa.aaM-C0C0C QSFP+ AOC is a 4-channel active optical cable for 40G Ethernet applications that is designed to meet the QSFP+ 10Gbps 4X Pluggable Transceiver SFF-8436 specification. This full-duplex optical assembly offers 4 independent transmit and receive channels, each capable of 10Gbps operation for an aggregate bandwidth of 40Gbps.
The cables use the standard multimode fiber cable carrying a nominal wavelength of 850nm. The electrical interface uses a standard 38 contact edge type connector and is electrically compliant with the SFI+ and PPI interface supporting Infiniband, Ethernet, Fiber Channel. The connector is hot pluggable and provides I2C serials access via an on-board microcontroller. QSFP+ AOC can be used as a direct replacement for traditional copper cables with the added benefit of a lighter weight and smaller diameter solution for cable lengths from 1 to 300 meters.

Product Features

- 4 high-speed full duplex channels
- QSFP+ MSA compliant
- Built-in digital diagnostic functions
- Hot-pluggable QSFP+ footprint
- Cable lengths from 1 to 300 meters
- Low power consumption, less than 1.3W
- RoHS Compliant
- Operating temperature range: 0°C to70°C

Applications

- 40G Ethernet
- Infiniband interconnects

Ordering Information

Part Number	Description	Color on Clasp
AOC-QSFP10-QSFP10-OM3-aaa.aaM-C0C0C	40G QSFP+ Active Optical Cable (length from 1m to 300m)	Blue

For More Information:
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General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Bit Error Rate	BER			10^{-12}		
Operating Temperature	T_C	0		70	°C	1
Storage Temperature	T_{STO}	-40		85	°C	2
Input Voltage	V_{CC}	3.14	3.3	3.46	V	
Maximum Voltage	V_{MAX}	-0.5		3.6	V	3

Notes:
1. Case temperature
2. Ambient temperature
3. For electrical power interface

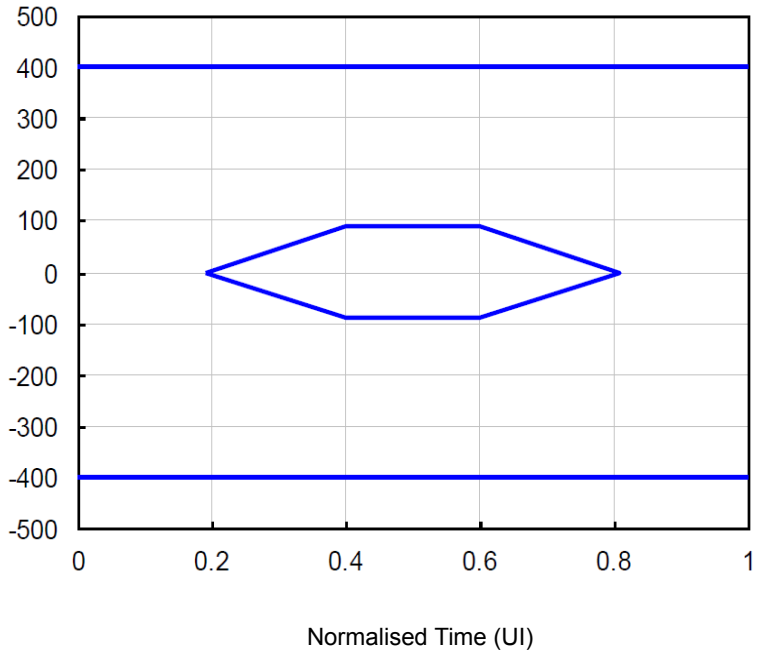
Link Distances

Data Rate	Fiber Type	Distance Range (m)
40 Gb/s	OM3 MMF	Up to 300

AOC Electrical Input Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR		10.3125	10.5	Gb/s	
Differential Data Input Swing	V_{IN_PP}	180		1200	mV	
Single Ended Voltage Tolerance	V	-0.3		3.8	V	
AC Common Mode Voltage	V_{CM}			25	mV	
Total Jitter (p-p)	TJ			0.4	UI	
Deterministic Jitter (p-p)	DJ			0.15	UI	
Eye Mask						1

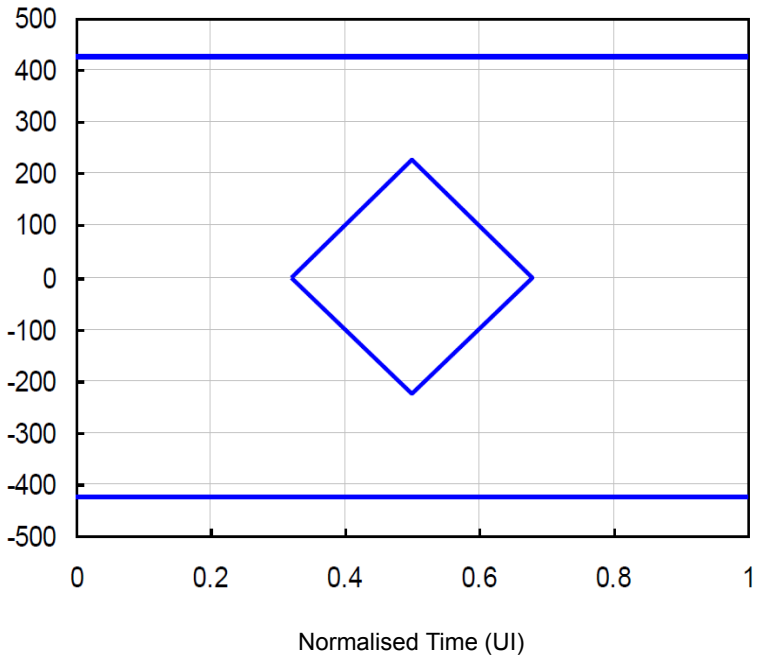
Notes:
1. The worst case electrical input is defined by the eye mask:



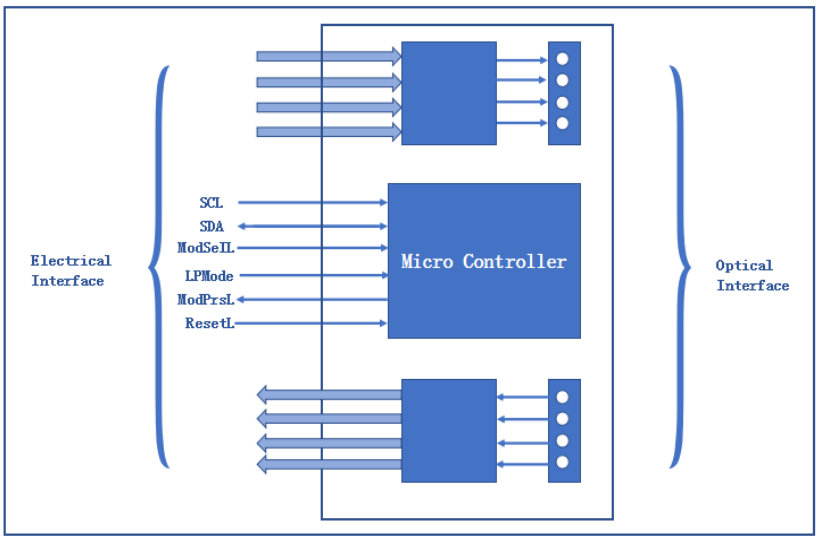
AOC Electrical Output Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR		10.3125	10.5	Gb/s	
Differential Data Output Swing	V_{OUT_PP}	340		800	mV	
Differential Data Output Swing in Squelched State	V_{OUT_sq}			50	mV	
Single Ended Voltage Tolerance	V	-0.3		3.8	V	
Output AC Common Mode Voltage	V_{CM}			15	mV	1
Data Output Rise Time /Fall Time(20%-80%)	t_r/ t_f	28			ps	
Total Jitter (p-p)	TJ			0.7	UI	
Deterministic Jitter (p-p)	DJ			0.4	UI	
Eye Mask						2

Notes:
1. RMS
2. The worst case electrical output is defined by the eye mask:



Block-Diagram-of-Transceiver



Functions Description

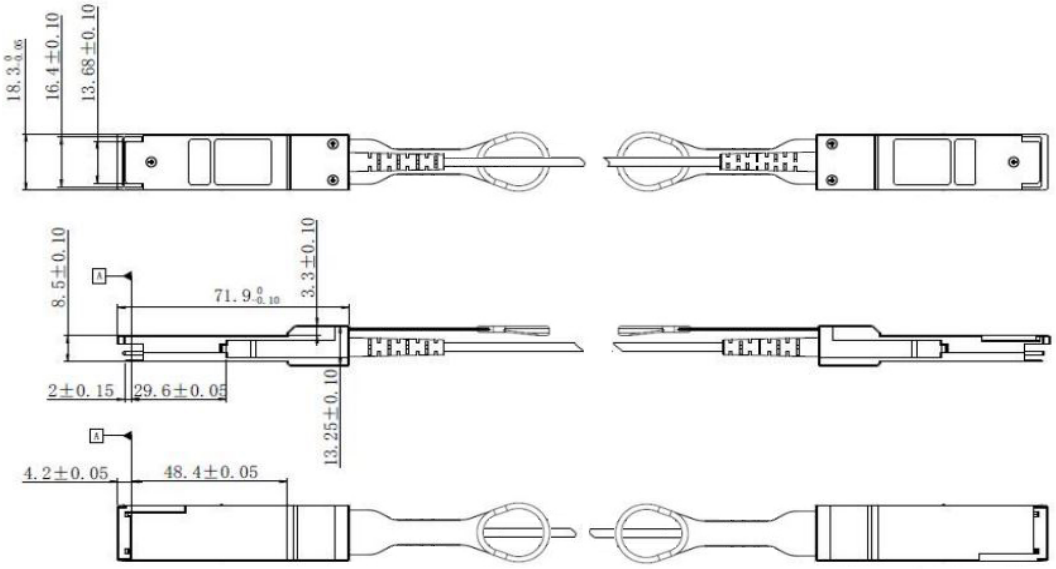
The QSFP AOC has miniature optical engines embedded into each end of the cable assembly. The engines interconnect 4 independent transmit/receive lanes.

A functional block diagram of the engine is shown in the above figure. The transmitter section consists of a 4-channel VCSEL array, a 4-channel input buffer and laser driver.

An on board micro-controller provides control, diagnostic and monitoring for the cable functions, as well as the external I2C serial communication interface.

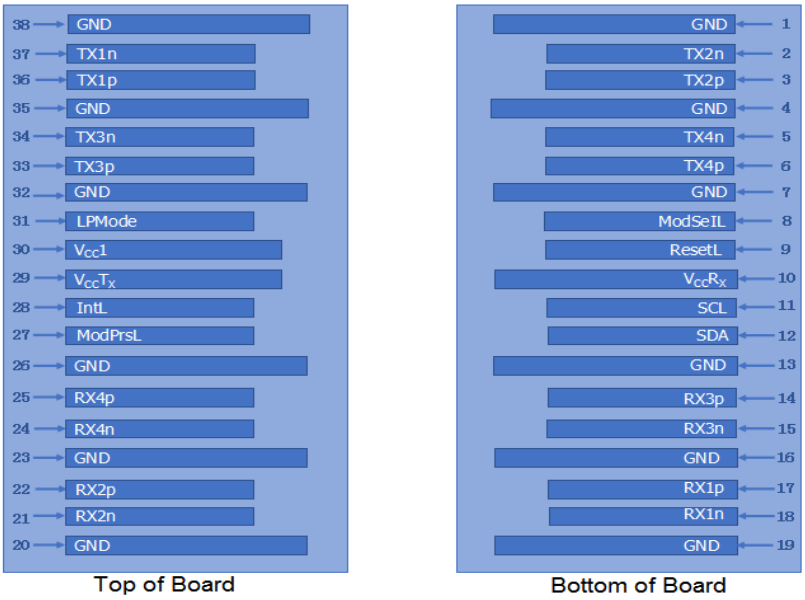
The receiver section consists of a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel output buffer.

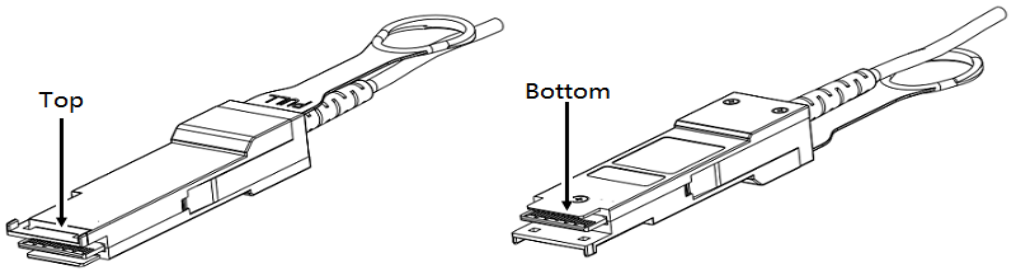
Dimensions



ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED
UNIT: mm

Electrical Pad Layout





Pin Assignment

PIN #	Symbol	Description	Remarks
1	GND	Ground	5
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	5
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	5
8	ModSelL	Module Insertion Indicator Pin	1
9	ResetL	Module Reset	2
10	$V_{cc}R_X$	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	5
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	5
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	5
20	GND	Ground	5
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	5
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	5
27	ModPrsL	Module Present	3
28	IntL	Interrupt	4
29	$V_{cc}T_X$	+3.3V Power Supply transmitter	
30	V_{cc1}	+3.3V Power Supply	
31	LPMode	Low Power Mode	5
32	GND	Ground	5
33	Tx3p	Transmitter Non-Inverted Data Input	

34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	5
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	5

Notes:
1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL is High, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module
2. The module restart pin, when the low level on the ResetL pin lasts longer than the minimum pulse length, resets the module and restores all user modules to their default state. When performing reset device, the host should ignore all status bits. Until the module reset interrupt is completed, please note that during hot plugging, the module will issue this information to complete the reset interrupt without resetting
3. This pin is active high, indicating that the module is running under a low power module.
4. IntL is the output pin, which is the open collector output and must be pulled up to Vcc on the motherboard. When it is low, it indicates that the module may malfunction. The host uses a 2-wire serial interface to identify the interrupt source
5.Circuit ground is internally isolated from chassis ground.

References

1. IEEE standard 802.3ba. IEEE Standard Department, 2010.
2. QSFP+ 10Gbps 4X PLUGGABLE TRANSCEIVER –SFF-8436