DATA SHEET

MODULETEK:AOC-QSFP10-QSFP10-OM3-aaa.aaM-D0D0C

40Gb/s QSFP+ Active Optical Cable

AOC-QSFP10-QSFP10-OM3-aaa.aaM-D0D0C Overview

ModuleTek’ s AOC-QSFP10-QSFP10-OM3-aaa.aaM-D0D0C QSFP+ AOC is a 4-channel active optical cable for 40G Ethernet applications that is designed to meet the QSFP+ 10Gbps 4X Pluggable Transceiver SFF-8436 specification. This full-duplex optical assembly offers 4 independent transmit and receive channels, each capable of 10Gbps operation for an aggregate bandwidth of 40Gbps.
The cables use the standard multimode fiber cable carrying a nominal wavelength of 850nm. The electrical interface uses a standard 38 contact edge type connector and is electrically compliant with the SFI+ and PPI interface supporting Infiniband, Ethernet, Fiber Channel. The connector is hot pluggable and provides I2C serials access via an on-board microcontroller. QSFP+ AOC can be used as a direct replacement for traditional copper cables with the added benefit of a lighter weight and smaller diameter solution for cable lengths from 1 to 300 meters.

Product Features

- 4 high-speed full duplex channels
- QSFP+ MSA compliant
- Built-in digital diagnostic functions
- Hot-pluggable QSFP+ footprint
- Cable lengths from 1 to 300 meters
- Low power consumption, less than 1.3W
- RoHS Compliant
- Operating temperature range: 0°C to 70°C

Applications

- 40G Ethernet
- Infiniband interconnects

Ordering Information

Part Number	Description	Color on Clasp
AOC-QSFP10-QSFP10-OM3-aaa.aaM-D0D0C	40G QSFP+ Active Optical Cable (length from 1m to 300m)	maize-yellow

For More Information:
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Email: sales@moduletek.com

General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Bit Error Rate	BER			10^{-12}		
Operating Temperature	T_C	0		70	°C	1
Storage Temperature	T_{STO}	-40		85	°C	2
Input Voltage	V_{CC}	3.14	3.3	3.46	V	
Maximum Voltage	V_{MAX}	-0.5		3.6	V	3
Minimum bending radius	R	30			mm	
The weight of module	G		98.5		g	4
Fiber Optical Cable Weight	G		5.8		g/M	5

Notes:
1. Case temperature
2. Ambient temperature
3. For electrical power interface
4. The weight of AOC-QSFP10-QSFP10-OM3-1M-D0D0C
5. The weight of fiber optical cable per unit length

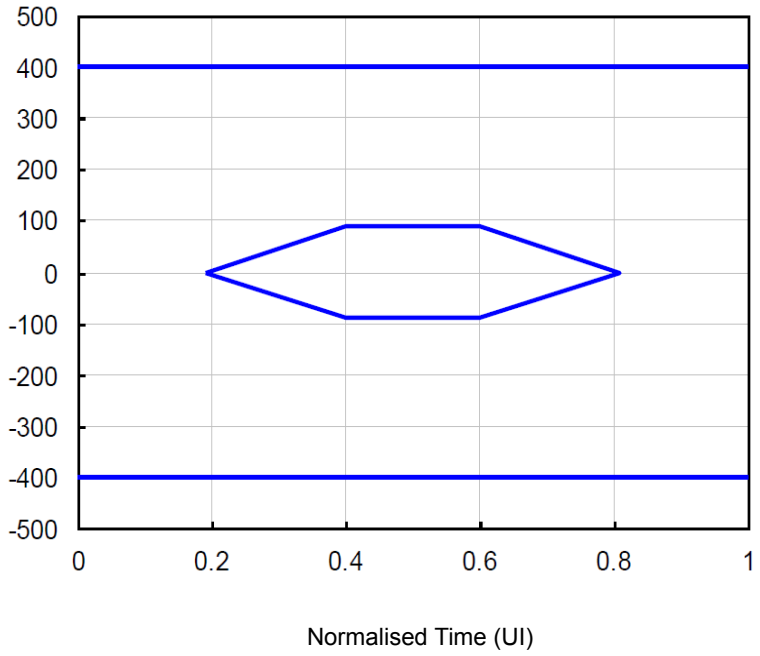
Link Distances

Data Rate	Fiber Type	Distance Range (m)
40 Gb/s	OM3 MMF	Up to 300

AOC Electrical Input Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR		10.3125	10.5	Gb/s	
Differential Data Input Swing	V_{IN_PP}	180		1200	mV	
Single Ended Voltage Tolerance	V	-0.3		3.8	V	
AC Common Mode Voltage	V_{CM}			25	mV	
Total Jitter (p-p)	TJ			0.4	UI	
Deterministic Jitter (p-p)	DJ			0.15	UI	
Eye Mask						1

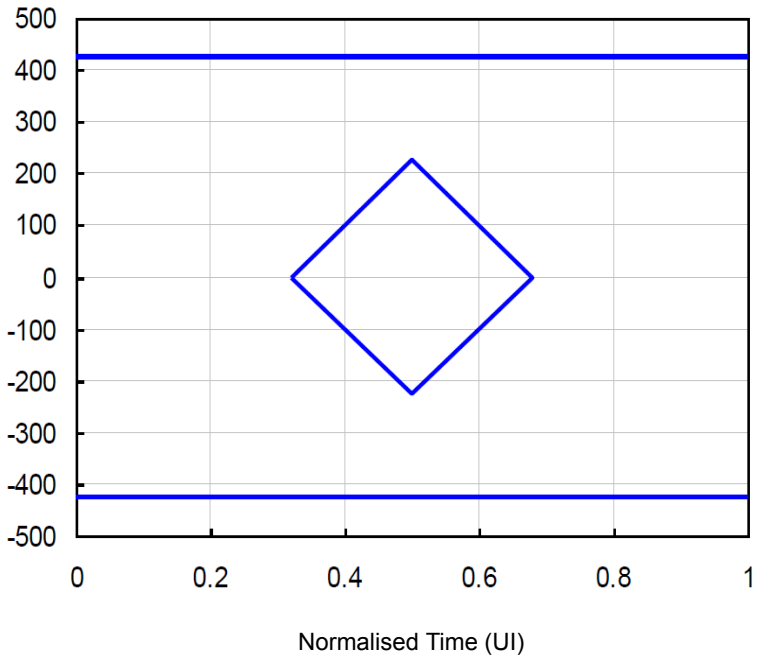
Notes:
1. The worst case electrical input is defined by the eye mask:



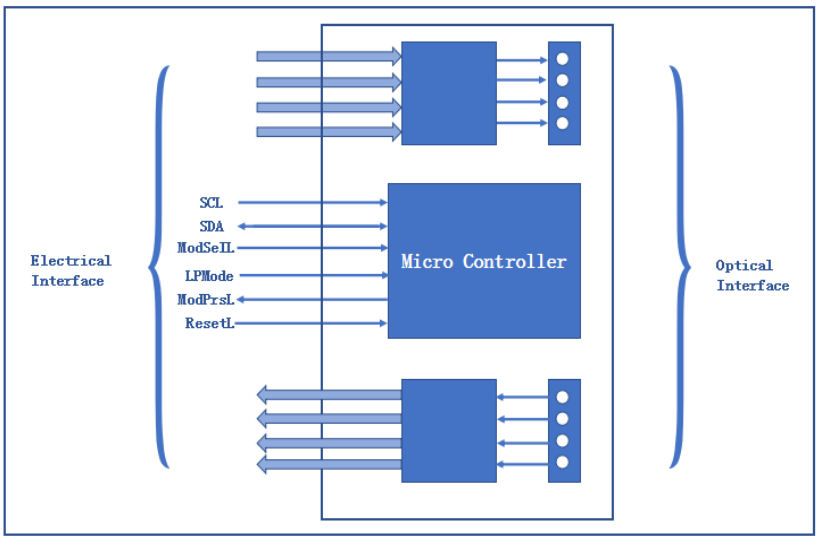
AOC Electrical Output Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR		10.3125	10.5	Gb/s	
Differential Data Output Swing	V_{OUT_PP}	340		800	mV	
Differential Data Output Swing in Squelched State	V_{OUT_sq}			50	mV	
Single Ended Voltage Tolerance	V	-0.3		3.8	V	
Output AC Common Mode Voltage	V_{CM}			15	mV	1
Data Output Rise Time /Fall Time(20%-80%)	t_r/ t_f	28			ps	
Total Jitter (p-p)	TJ			0.7	UI	
Deterministic Jitter (p-p)	DJ			0.4	UI	
Eye Mask						2

Notes:
1. RMS
2. The worst case electrical output is defined by the eye mask:



Block-Diagram-of-Transceiver



Functions Description

The QSFP AOC has miniature optical engines embedded into each end of the cable assembly. The engines interconnect 4 independent transmit/receive lanes.

A functional block diagram of the engine is shown in the above figure. The transmitter section consists of a 4-channel VCSEL array, a 4-channel input buffer and laser driver.

An on board micro-controller provides control, diagnostic and monitoring for the cable functions, as well as the external I2C serial communication interface.

The receiver section consists of a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel output buffer.

Digital Diagnostic Functions

The AOC-QSFP10-QSFP10-OM3-aaa.aaM-D0D0C supports the 2-wire serial communication protocol defined in SFF-8436, which accesses digital diagnostic information via a 2-wire interface at address 0xA2. Digital diagnostics default to internal calibration, and the internal micro-control unit accesses device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power, and transceiver supply voltage in real time. The module implements the alarm function of the SFF-8436, alerts the user when a particular operating parameter exceeds the factory-set normal range.

Digital Diagnostic Threshold Range				
Parameter	**High Alarm(HEX)**	**High Warning(HEX)**	**Low Warning(HEX)**	**Low Alarm(HEX)**
Temperature(°C)	75(0x5500)	70(0x4600)	0(0x0000)	-5(0xF600)
Voltage(V)	3.63(0x8DCC)	3.46(0x8728)	3.13(0x7A44)	2.97(0x7404)
Bias Current(mA)	15(0x1D4C)	12(0x1770)	2(0x03E8)	1(0x01F4)
Tx Power(dBm)	3.192(0x5175)	2.4(0x43E2)	-7.6(0x06C9)	-8.57(0x056E)
Rx Power(dBm)	5.41(0x87C4)	2.4(0x43E2)	-9.5(0x0462)	-12.51(0x0231)

A0 Write Protection

Security Level 1 Password		
Password Entry ADDr	**Size**	**Vaules(HEX)**
Page A0，7BH-7EH	4	00 00 00 00

MODULETEK's AOC-QSFP10-QSFP10-OM3-aaa.aaM-D0D0C has the A0 write protection function. The user can enter the security level 1 working state and write the contents of Table 00 and Table 01 of the device address A0H of the module. The method to enter the working state of security level 1 is to write the security level 1 password in order in the 7BH-7EH registers of A0h of the module. After entering security level 1, the user can directly write to the contents of the A0H device address, or modify the contents of the A0H 7F table selection register to write to the contents of Table 00 or Table 02. This version of the module does not support users to modify the password of security level 1. If you need to modify the security level 1 password, you must notify our company to modify it before shipping.

IIC Memory Map(Page A0 HEX, Unlisted Fields are Blank/Empty

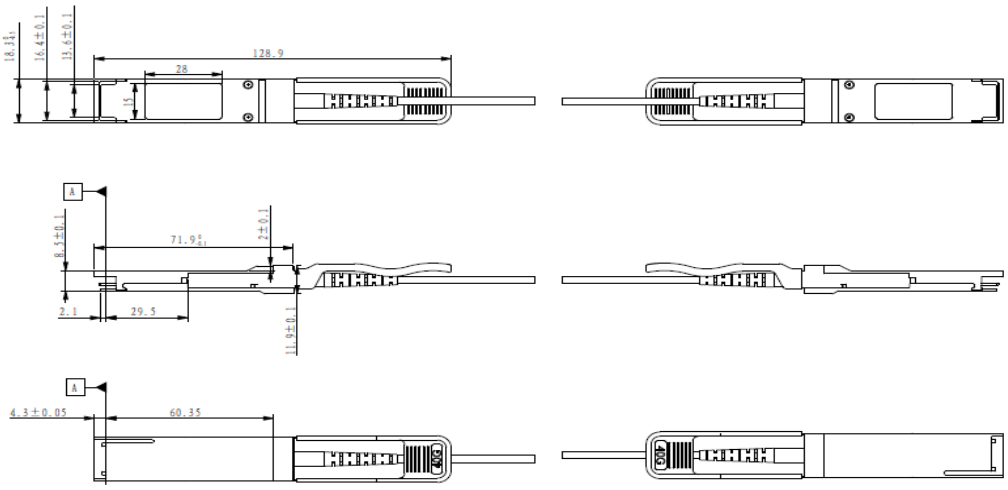
IIC ADDr	Size	Name	Description	Vaules(HEX)
0	1	Identifier	QSFP+	0D
1-2	2	Status	bit0:Data Not Ready; bit1:IntL; bit2: Flat mem	00 00
3	1	Channel Status LOS Flag	Latched TX/RX LOS indicator	00
4	1	Channel Status TxFault Flag	Latched TX fault indicator	00
5	1	Channel Status Reserved5	Reserved	00

6	1	Module Monitor Temp AW Flag	Latched temperature alarm/ warning and initialization complete	00
7	1	Module Monitor Vcc AW Flag	Latched Vcc alarm/warning	00
8	1	Module Monitor Reserved8	Reserved	00
9-10	2	Channel Mon RxPower AW Flag	Latched Rx Power alarm/ warning	00 00
11-12	2	Channel Mon TxBias AW Flag	Latched Tx Bias alarm/ warning	00 00
13-21	9	Channel Mon Reserved13	Reserved	00
22-23	2	Module Monitor Temp	Internally measured module temperature	00 00
24-25	2	Module Monitor Reserved24	Reserved	00 00
26-27	2	Module Monitor Voltage	Internally measured module supply voltage	00 00
28-33	6	Module Monitor Reserved28	Reserved	00
34-35	2	Channel Mon Rx1Power	Internally measured RX input power, channel 1	00 00
36-37	2	Channel Mon Rx2Power	Internally measured RX input power, channel 2	00 00
38-39	2	Channel Mon Rx3Power	Internally measured RX input power, channel 3	FF FF
40-41	2	Channel Mon Rx4Power	Internally measured RX input power, channel 4	FF FF
42-43	2	Channel Mon Tx1Bias	Internally measured TX bias, channel 1	00 00
44-45	2	Channel Mon Tx2Bias	Internally measured TX bias, channel 2	00 00
46-47	2	Channel Mon Tx3Bias	Internally measured TX bias, channel 3	00 00
48-49	2	Channel Mon Tx4Bias	Internally measured TX bias, channel 4	00 00
50-57	32	Channel Mon TX Power	Internally measured TX power	00
58-81	32	Channel Mon Reserved50	Reserved	FF FF
82-85	4	Reserved82	Reserved	FF

86	1	Control TxDisable	Txn Read/write bit that allows software disable of transmitters	00
87	1	Control Rx Rate Select	Rx channel Software Rate Select	00
88	1	Control Tx Rate Select	Tx channel Software Rate Select	00
89	1	Control Rx4 App Select	Software Application Select per SFF-8079, Rx Channel 4 (Optional)	00
90	1	Control Rx3 App Select	Software Application Select per SFF-8079, Rx Channel 3 (Optional)	00
91	1	Control Rx2 App Select	Software Application Select per SFF-8079, Rx Channel 2 (Optional)	00
92	1	Control Rx1 App Select	Software Application Select per SFF-8079, Rx Channel 1 (Optional)	00
93	1	Control Power	Power set to low power mode/ Override of LPMode signal setting the power mode with software	00
94	1	Control Tx4 App Select	Software Application Select per SFF-8079, Tx Channel 4 (Optional)	00
95	1	Control Tx3 App Select	Software Application Select per SFF-8079, Tx Channel 3 (Optional)	00
96	1	Control Tx2 App Select	Software Application Select per SFF-8079, Tx Channel 2 (Optional)	00
97	1	Control Tx1 App Select	Software Application Select per SFF-8079, Tx Channel 1 (Optional)	00
98-99	2	Control Reserved98	Reserved	FF FF
100	1	Mask TxRx LOS	Masking bit for TX/RX LOS indicator	00
101	1	Mask TxFault	Masking bit for TX fault indicator	00
102	1	Mask Reserved102	Reserved	FF
103	1	Mask Temp AW	Masking bit for Temperature alarm/warning and initialization complete	00

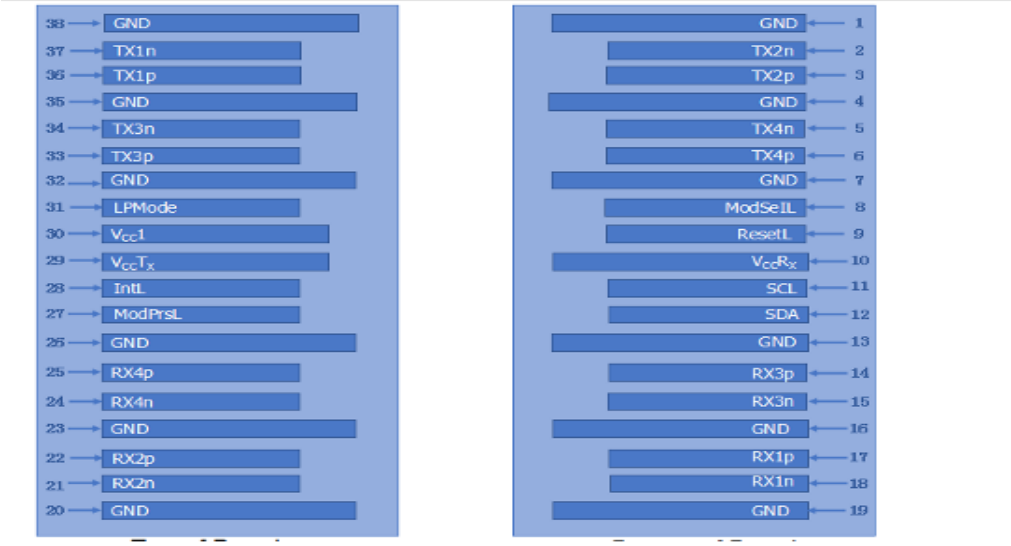
104	1	Mask Vcc AW	Masking bit for Vcc alarm/ warning	00
105-106	2	Mask Reserved105	Reserved	FF FF
107-118	12	Reserved107	Reserved	FF
119-122	4	Password Change Entry Area	Password Change Entry Area (optional)	00 00 00 00
123-126	4	Password Entry Area	Password Entry Area (Optional)	00 00 00 00
127	1	Page Select	Page Select Byte	00

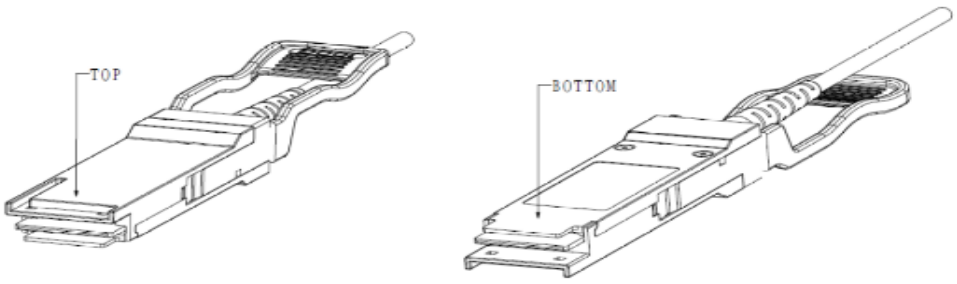
外形尺寸



未注尺寸公差 ±0.2mm
单位：毫米

引脚图


38 GND
37 TX1n
36 TX1p
35 GND
34 TX3n
33 TX3p
32 GND
31 LPMode
30 Vcc1
29 VccTx
28 IntL
27 ModPrsL
26 GND
25 RX4p
24 RX4n
23 GND
22 RX2p
21 RX2n
20 GND
GND 1
TX2n 2
TX2p 3
GND 4
TX4n 5
TX4p 6
GND 7
ModSelL 8
ResetL 9
VccRx 10
SCL 11
SDA 12
GND 13
RX3p 14
RX3n 15
GND 16
RX1p 17
RX1n 18
GND 19


TOP
BOTTOM

Pin Assignment

PIN #	Symbol	Description	Remarks
1	GND	Ground	5
2	Tx2n	Transmitter Inverted Data Input, LAN2	
3	Tx2p	Transmitter Non-Inverted Data Input, LAN2	
4	GND	Ground	5
5	Tx4n	Transmitter Inverted Data Input, LAN4	
6	Tx4p	Transmitter Non-Inverted Data Input, LAN4	
7	GND	Ground	5
8	ModSelL	Module select pin, the module responds to two-wire serial communication when low level	1
9	ResetL	Module Reset	2
10	$V_{cc}R_X$	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	5
14	Rx3p	Receiver Non-Inverted Data Output, LAN3	
15	Rx3n	Receiver Inverted Data Output, LAN3	
16	GND	Ground	5
17	Rx1p	Receiver Non-Inverted Data Output, LAN1	
18	Rx1n	Receiver Inverted Data Output, LAN1	
19	GND	Ground	5
20	GND	Ground	5
21	Rx2n	Receiver Inverted Data Output, LAN2	
22	Rx2p	Receiver Non-Inverted Data Output, LAN2	
23	GND	Ground	5
24	Rx4n	Receiver Inverted Data Output, LAN4	
25	Rx4p	Receiver Non-Inverted Data Output, LAN4	
26	GND	Ground	5
27	ModPrsL	The module is inserted into the indicate pin and grounded in the module.	3
28	IntL	Interrupt	4
29	$V_{cc}T_X$	+3.3V Power Supply transmitter	
30	V_{cc1}	+3.3V Power Supply	
31	LPMode	Low Power Mode	5
32	GND	Ground	5

33	Tx3p	Transmitter Non-Inverted Data Input, LAN3	
34	Tx3n	Transmitter Inverted Data Input, LAN3	
35	GND	Ground	5
36	Tx1p	Transmitter Non-Inverted Data Input, LAN1	
37	Tx1n	Transmitter Inverted Data Input, LAN1	
38	GND	Ground	5

Notes:
1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL is High, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module
2. The module restart pin, when the low level on the ResetL pin lasts longer than the minimum pulse length, resets the module and restores all user modules to their default state. When performing reset device, the host should ignore all status bits. Until the module reset interrupt is completed, please note that during hot plugging, the module will issue this information to complete the reset interrupt without resetting
3. This pin is active high, indicating that the module is running under a low power module.
4. IntL is the output pin, which is the open collector output and must be pulled up to Vcc on the motherboard. When it is low, it indicates that the module may malfunction. The host uses a 2-wire serial interface to identify the interrupt source
5.Circuit ground is internally isolated from chassis ground.

References

1. IEEE standard 802.3ba. IEEE Standard Department, 2010.
2. QSFP+ 10Gbs 4X PLUGGABLE TRANSCEIVER –SFF-8436