# DATA SHEET

## MODULETEK: DAC-QSFP10-QSFP10-A-M-xxAWG-aa.aaM-C0C0C

QSFP+ Active Copper Cable Assembly

## DAC-QSFP10-QSFP10-A-M-xxAWG-aa.aaM-C0C0C Overview

ModuleTek's DAC-QSFP10-QSFP10-A-M-xxAWG-aa.aaM-C0C0C QSFP+ (Quad Small Form-factor Pluggable Plus) active direct-attach copper cables are suitable for very short distances and offer a highly cost-effective way to establish a 40-Gigabit link between QSFP+ ports. QSFP+ are designed for a high density cabling interconnect system capable of delivering an aggregate data bandwidth of 40Gbps. This interconnect system is fully compliant with QSFP+ MSA. The QSFP+ cables support the bandwidth transmission requirements defined by IEEE802.3ba (40Gbps).

## Product Features

- Up to 40 Gb/s bi-directional data links
- Compliant with QSFP+ MSA specifications
- Fully Compliant with IEEE802.3ba and Infiniband QDR specifications
- 4 independent duplex channels operating at 10Gbps, also support for 2.5Gbps,5Gbps data rates
- All-metal housing for superior EMI performance
- Single power supply 3.3V
- low power consumption, less than 1.5W
- RoHS Compliant
- Operating temperature range: 0°C to 70°C

## Applications

- 40Gigabit Ethernet
- Serial Data Transmission
- QDR

## Ordering Information

| Part Number | Description | Gauge | Length |
|---|---|---|---|
| DAC-QSFP10-QSFP10-A-M-xxAWG-aa.aaM-C0C0C | QSFP+ 40G Active Copper Cable Assembly, aa.aa≤7 | 30AWG | ≤7m |
| DAC-QSFP10-QSFP10-A-M-xxAWG-aa.aaM-C0C0C | QSFP+ 40G Active Copper Cable Assembly, 7<aa.aa≤10 | 28AWG | 7m<length≤10m |

**Note:**
1. “A” indicates active cable
2. “M” indicates built-in MCU
3. “aa.aa” indicates the cable length in meters.
4. The wire diameter of the products in the above list is the default value under different lengths. We can also provide other wire products to customers with special requirements.

**For More Information:**
ModuleTek Limited
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Email: sales@moduletek.com

## General Specifications

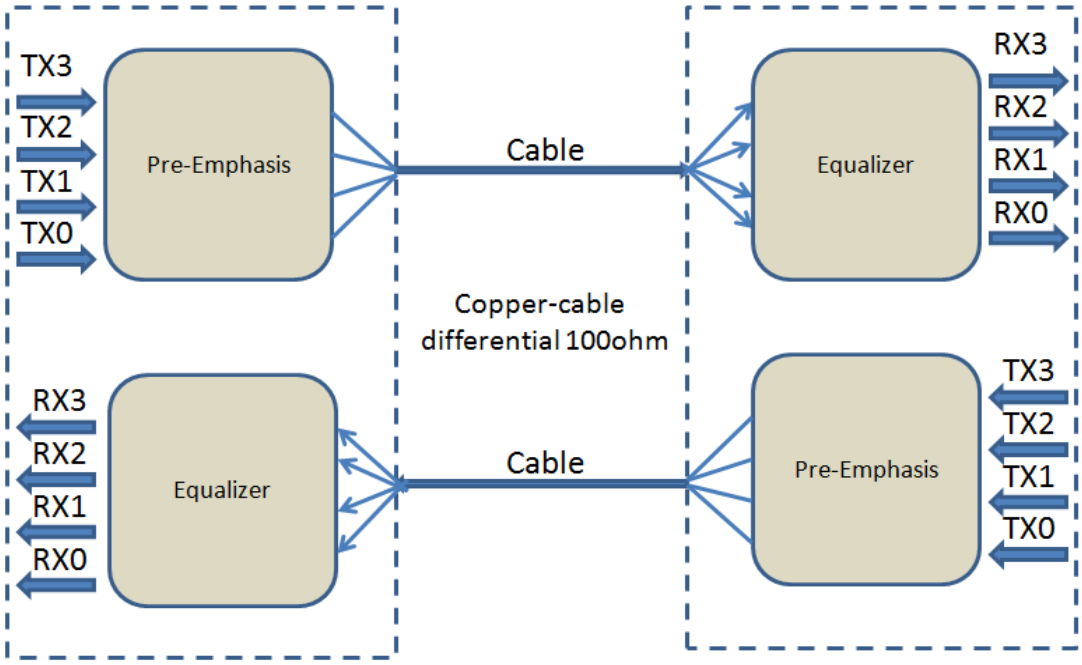
| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Bit Error Rate | BER | | | $10^{-12}$ | | |
| Operating Temperature | $T_C$ | 0 | | 70 | °C | 1 |
| Storage Temperature | $T_{STO}$ | -40 | | 85 | °C | 2 |
| Input Voltage | $V_{CC}$ | 3.14 | 3.3 | 3.46 | V | |

**Notes:**
1.Case temperature
2.Ambient temperature

## Cable Specifications

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Wire Gauge | | 30AWG | | 28AWG | AWG | |
| Cable Impedance | Z | 90 | 100 | 110 | Ohm | |

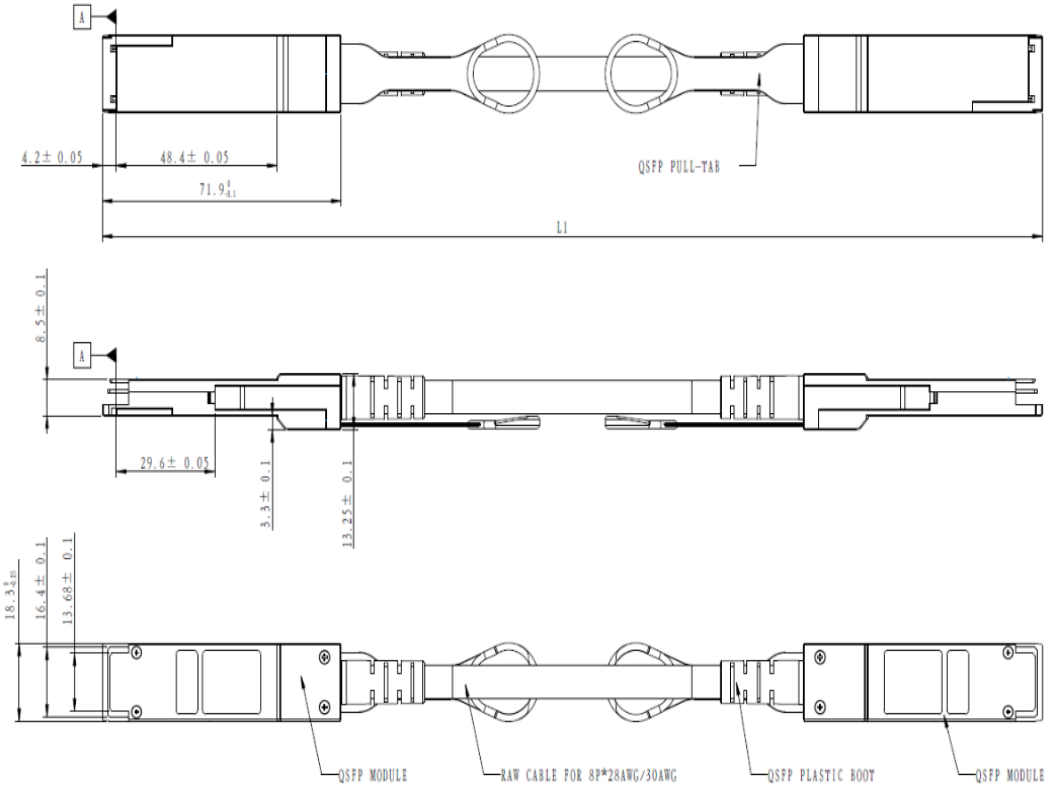
## Block Diagram of Transceiver




## Functions Description

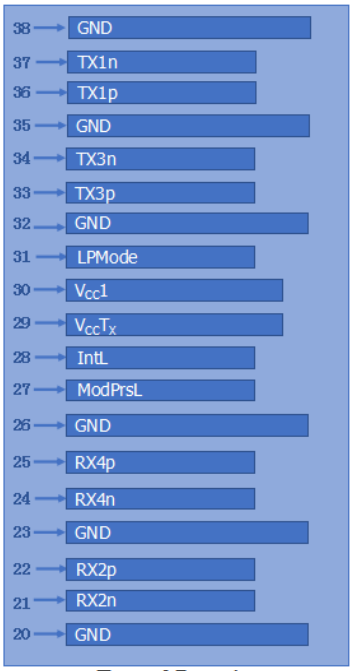
The transmitter side accepts electrical input signals. All input data signals are differential LVPECL or CML logic and they are internally terminated. The parallel input electrical signal first is processed via the Pre-Emphasis.At the receiver side, the parallel electrical signals is recovered via Equalizer. The outputs electrical signals of receive side are voltage compatible with Current Mode Logic (CML) levels. All data signals are differential and support a data rate up to 10Gbps per channel. All transmitter signals and receiver signals are AC coupled internally on both modules ends.Active cable assembly has built-in MCU, offer a number of additional host-management capabilities. I2C (Inter-IC bus protocol) interface and on-board EEPROM features enable the host to detect or configure specific performance characteristics.

## Dimensions

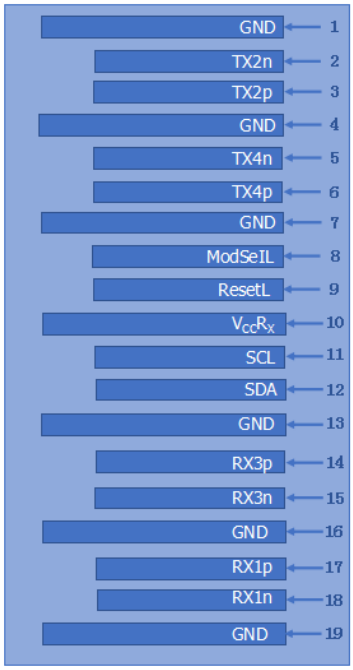



ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED
UNIT: mm

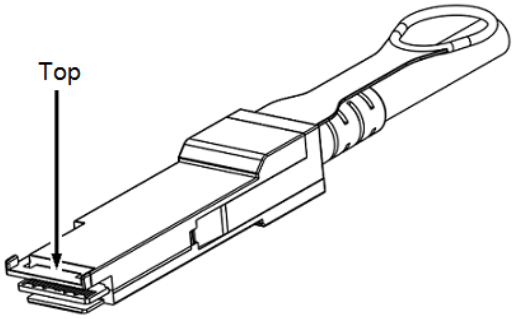
## Electrical Pad Layout

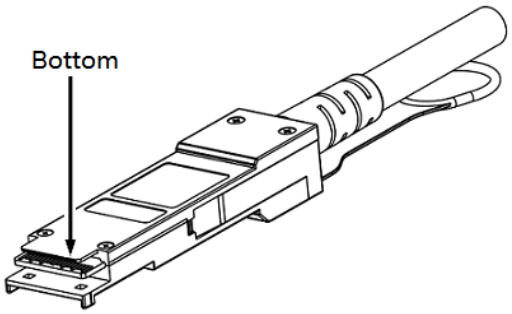



Top of Board




Bottom of Board



## Pin Assignment

| PIN # | Symbol | Description | Remarks |
|---|---|---|---|
| 1 | GND | Ground | 5 |
| 2 | Tx2n | Transmitter Inverted Data Input | |
| 3 | Tx2p | Transmitter Non-Inverted Data Input | |
| 4 | GND | Ground | 5 |
| 5 | Tx4n | Transmitter Inverted Data Input | |
| 6 | Tx4p | Transmitter Non-Inverted Data Input | |
| 7 | GND | Ground | 5 |
| 8 | ModSelL | Module Insertion Indicator Pin | 1 |
| 9 | ResetL | Module Reset | 2 |
| 10 | $V_{cc}R_X$ | +3.3V Power Supply Receiver | |
| 11 | SCL | 2-wire serial interface clock | |
| 12 | SDA | 2-wire serial interface data | |
| 13 | GND | Ground | 5 |
| 14 | Rx3p | Receiver Non-Inverted Data Output | |
| 15 | Rx3n | Receiver Inverted Data Output | |
| 16 | GND | Ground | 5 |
| 17 | Rx1p | Receiver Non-Inverted Data Output | |
| 18 | Rx1n | Receiver Inverted Data Output | |
| 19 | GND | Ground | 5 |
| 20 | GND | Ground | 5 |
| 21 | Rx2n | Receiver Inverted Data Output | |
| 22 | Rx2p | Receiver Non-Inverted Data Output | |
| 23 | GND | Ground | 5 |
| 24 | Rx4n | Receiver Inverted Data Output | |
| 25 | Rx4p | Receiver Non-Inverted Data Output | |
| 26 | GND | Ground | 5 |
| 27 | ModPrsL | Module Present | 3 |
| 28 | IntL | Interrupt | 4 |
| 29 | $V_{cc}T_X$ | +3.3V Power Supply transmitter | |
| 30 | $V_{cc1}$ | +3.3V Power Supply | |
| 31 | LPMode | Low Power Mode | 5 |
| 32 | GND | Ground | 5 |
| 33 | Tx3p | Transmitter Non-Inverted Data Input | |

| | | | |
|---|---|---|---|
| 34 | Tx3n | Transmitter Inverted Data Input | |
| 35 | GND | Ground | 5 |
| 36 | Tx1p | Transmitter Non-Inverted Data Input | |
| 37 | Tx1n | Transmitter Inverted Data Input | |
| 38 | GND | Ground | 5 |

**Notes:**
1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL is High, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module
2. The module restart pin, when the low level on the ResetL pin lasts longer than the minimum pulse length, resets the module and restores all user modules to their default state. When performing reset device, the host should ignore all status bits. Until the module reset interrupt is completed, please note that during hot plugging, the module will issue this information to complete the reset interrupt without resetting
3. This pin is active high, indicating that the module is running under a low power module.
4. IntL is the output pin, which is the open collector output and must be pulled up to Vcc on the motherboard. When it is low, it indicates that the module may malfunction. The host uses a 2-wire serial interface to identify the interrupt source
5.Circuit ground is internally isolated from chassis ground.

## References

1. IEEE standard 802.3ba. IEEE Standard Department.
2. QSFP+ 10Gbps 4X PLUGGABLE TRANSCEIVER –SFF-8436.