

DATA SHEET

MODULETEK-QSFP10-SR-C10

40Gb/s QSFP+ SR4 Transceiver

QSFP10-SR-C10 Overview

ModuleTek's QSFP10-SR-C10 QSFP+ SR4 optical transceivers are based on Ethernet IEEE P802.3ba standard and SFF-8436 standard. QSFP+ SR4 offers 4 independent transmit and receive channels, each capable of 10Gbps for an aggregate bandwidth of 40Gbps.

Product Features

- 4 high-speed full duplex channels
- Multi Rate, up to 10.5Gbps per channel
- QSFP+ MSA compliant
- Up to 100 meters over OM3 Multimode Fiber and 150 meters over OM4 Multimode Fiber
- Low power consumption, less than 1.5W
- Reliable VCSEL array technology
- Single 1X12 MPO receptacle
- RoHS Compliant
- Operating temperature range: 0°C to 70°C
- With digital diagnostic monitoring functions

Applications

- 40GBASE-SR4 40G Ethernet
- Breakout to four 10GBASE-SR Ethernet

Ordering Information

Part Number	Description	Color on Clasp
QSFP10-SR-C10	40G QSFP+ 850nm MPO Connectors, Up to 100m on OM3 MMF and 150m on OM4 MMF	Cream color
For More Information: ModuleTek Limited Web: www.moduletek.com Email: sales@moduletek.com		

General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Bit Error Rate	BER			10^{-12}		
Operating Temperature	T _{OP}	0		70	°C	1
Storage Temperature	T _{STO}	-40		85	°C	2
Input Voltage	V _{CC}	3.14	3.3	3.46	V	
Maximum Voltage	V _{MAX}	-0.5		3.6	V	3

Notes:

1. Case temperature
2. Ambient temperature
3. For electrical power interface

Optical-Characteristics-Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Average Launch Power (per lane)	P_{TX}	-7.6		2.4	dBm	
Optical Center Wavelength	λ_C	840		860	nm	
Extinction Ratio	ER	3			dB	
RMS Spectral Width	$\Delta\lambda$			0.65	nm	
Relative Intensity Noise	RIN			-128	dB/Hz	
Transmitter Dispersion Penalty	TDP			3.5	dB	
Transmitter Eye Mask						1
Launch Power of OFF Transmitter(per lane)	P_{OUT_OFF}			-30	dBm	2

Notes:

1. Compliant with IEEE 802.3ba
2. Average

Optical - Characteristics - Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Optical Center Wavelength	λ_C	840		860	nm	
Optical Input Power(per lane)	P_{RX}	-9.5		2.4	dBm	1
Damage Threshold	P	3.3			dBm	
Receiver Sensitivity (OMA)@10.3Gb/s	R_{X_SEN1}			-11.1	dBm	
Stressed Receiver Sensitivity in OMA, (per lane)				-7.5	dBm	
Receiver Reflectance	TR_{RX}			-12	dB	
LOS Assert	LOS_A	-25			dBm	
LOS De-Assert	LOS_D			-12	dBm	
LOS Hysteresis	LOS_H	0.5			dB	

Notes:

1. Average, Informative

Electrical - Characteristics - Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR			10.5	Gb/s	1
Differential data input swing	V_{IN_PP}	180		1200	mV	
Single Ended Input Voltage Tolerance	V	-0.3		3.8	mV	
Transmit Disable Voltage	V_D	$V_{CC}-1.3$		V_{CC}	V	
Transmit Enable Voltage	V_{EN}	V_{EE}		$V_{EE}+0.8$	V	

Notes:

1. Non-condensing

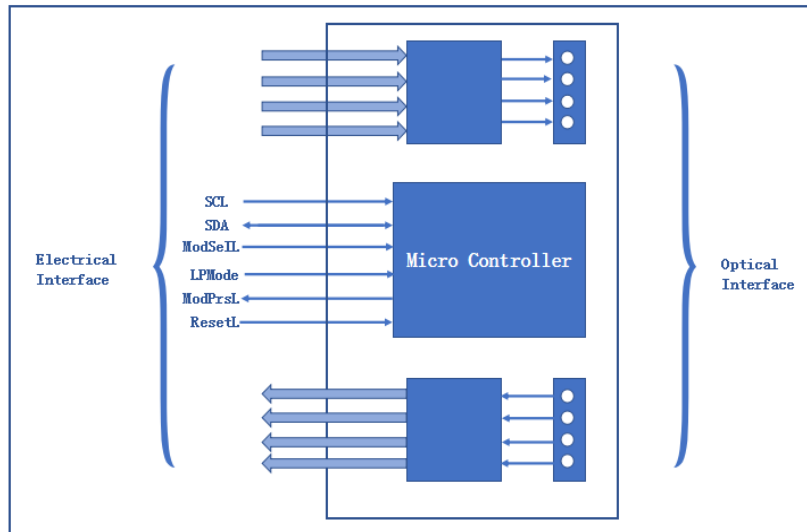
Electrical - Characteristics - Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR			10.5	Gb/s	
Differential Data Output Swing	V_{OUT_PP}	340		800	mV	
Differential Output Amplitude in Squelched state	V_{OUT_sq}			50	mV	
Single Ended Output Voltage Tolerance	V	-0.3		3.8	V	
Output AC Common Mode Voltage	V_{cm}			7.5	mV	1
Data Output Rise/Data Output Rise (20%-80%)	T_R/T_F	28			ps	
Total Jitter (p-p)	TJ			0.7	UI	
Deterministic Jitter (p-p)	DJ			0.4	UI	

Note:

- 1.RMS

Block-Diagram-of-Transceiver



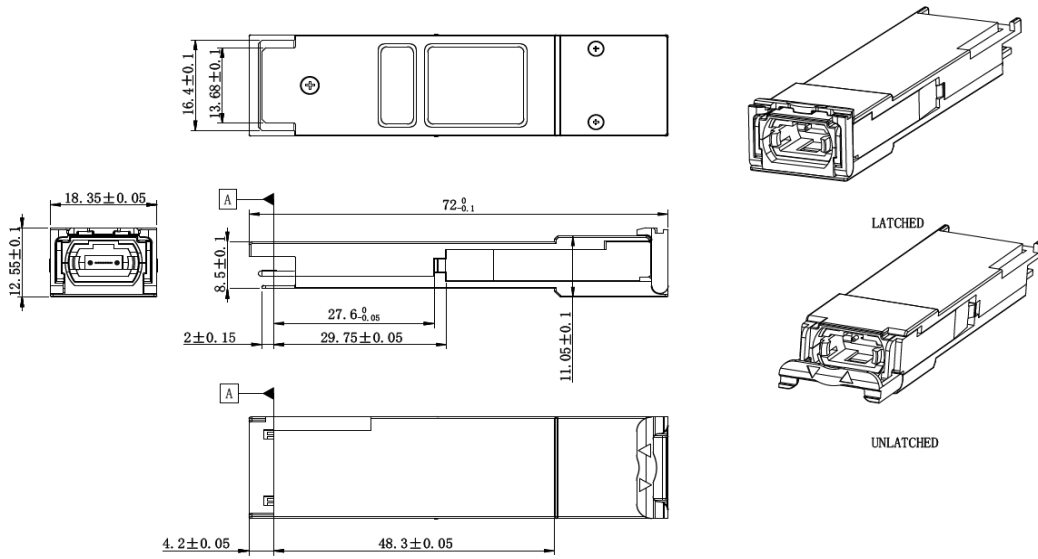
The QSFP-SR4 has miniature optical engine embedded into QSFP module. The engines interconnect 4 independent transmit/receive lanes.

A functional block diagram of the engine is shown in the above Figure. The transmitter sections consist of a 4-channel VCSEL array, a 4-channel input buffer and laser driver.

An on board micro-controller provides control, diagnostic and monitoring for the cable functions, as well as the external I2C serial communication interface.

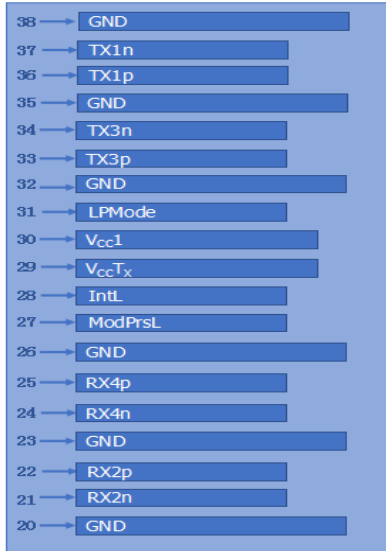
The Receiver section consists of a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel output buffer.

Dimensions

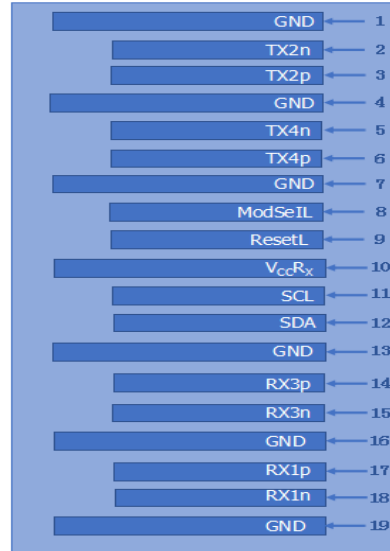


ALL DIMENSIONS ARE ± 0.2 mm UNLESS OTHERWISE SPECIFIED
UNIT: mm

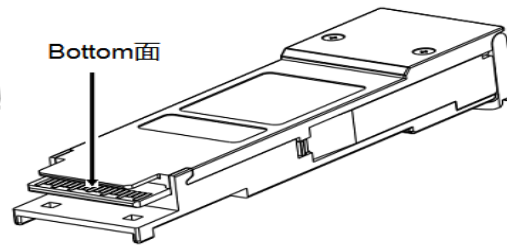
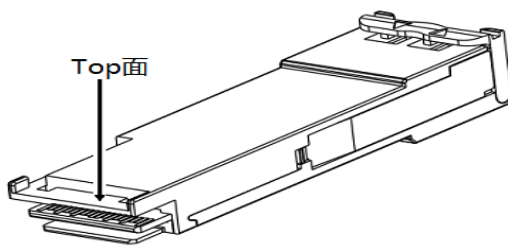
Electrical Pad Layout



Top of Board



Bottom of Board



Pin Assignment

PIN #	Symbol	Description	Remarks
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	V _{cc} R _X	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	V _{cc} T _X	+3.3V Power Supply transmitter	
30	V _{cc} 1	+3.3V Power Supply	
31	LPMMode	Low Power Mode	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	

35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	

References

1. IEEE standard 802.3ba. IEEE Standard Department, 2010.
2. QSFP+ 10Gbs 4X PLUGGABLE TRANSCEIVER –SFF-8436