DATA SHEET

MODULETEK: QSFP28-SR4-E10

100G QSFP28 SR4 Optical Transceiver

QSFP28-SR4-E10 Overview

ModuleTek's QSFP28-SR4-E10 QSFP28 SR4 optical transceivers are based on 100G Ethernet IEEE 802.3bm standard. QSFP28 SR4 offers 4 independent transmit and receive channels, each capable of 25G for an aggregate bandwidth of 100G.

Product Features

- Hot-pluggable QSFP28 package
- 4x25Gbps 850nm VCSEL laser
- Up to 103.1Gbps
- QSFP28 MSA compliant
- Up to 70m on OM3 Multimode Fiber and 100m on OM4 Multimode Fiber
- Single 1X12 MPO receptacle
- RoHS-6 Compliant
- Operating temperature range: 0°C to 70°C (case temperature)

Applications

- 100GBASE-SR4 100G Ethernet

Ordering Information

Part Number	Description	Color on Clasp
QSFP28-SR4-E10	100G QSFP28 850nm MPO Connectors, Up to 70m(OM3) or 100m(OM4) on MMF	beige

For More Information:
ModuleTek Limited
Web: www.moduletek.com
Email: sales@moduletek.com

General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Operating Temperature	T_C	0		70	°C	1
Storage Temperature	T_{STO}	-40		85	°C	2
Input Voltage	V_{CC}	3.14	3.3	3.46	V	
Maximum Voltage	V_{MAX}	-0.5		4	V	3

Notes:
1.Case temperature
2.Ambient temperature
3.For electrical power interface

Optical – Characteristics – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Signal rate(per lane)		25.78125±100ppm			Gbps	1
Optical Center Wavelength	λ_C	840	850	860	nm	
Spectral Width(RMS)	$\Delta\lambda$			0.60	nm	
Average Launch optical Power (per lane)	P_{TX}	-8.4		2.4	dBm	
Optical Modulation Amplitude(per lane)	OMA	-6.4		3	dBm	
Extinction Ratio	ER	2			dB	
Transmit optical power and TDEC difference	P-TDEC	-7.3			dBm	
Transmitter dispersion eye diagram closure	TDEC			4.3	dBm	
Launch Power of OFF Transmitter	P_{OUT_OFF}			-30	dBm	
Transmitter Eye Mask{X1,X2,X3,Y1,Y2,Y3}	{0.3,0.38,0.45,0.35,0.41,0.5}					2

Notes:
1.The module consists of 4 channels, and the data is the rate of per lane.
2.Hit Ratio 1.5x10^{-3} hits/sample

Optical – Characteristics – Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Signal rate(per lane)		25.78125±100ppm			Gbps	1
Optical Center Wavelength	λ_C	840		860	nm	
Average received optical power (per lane)	P_{RX}	-10.3		2.4	dBm	
Receive damage optical power input value	P	3.4			dBm	
Receiver Sensitivity (per lane)	R_{X_SEN}			-10.3	dBm	
Receiver Reflectance	TR_{RX}			-12	dB	
LOS Assert	LOS_A	-30			dBm	
LOS De-Assert	LOS_D			-13	dBm	
LOS Hysteresis	LOS_H	0.5	2		dB	

Notes:
1.The module consists of 4 channels, and the data is the rate of per lane.

General characteristics of the module

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data rate	BR			103.1	Gb/s	1
Bit error rate (no FEC forward error correction code)	BER			$5x10^{-5}$		2
Bit error rate (with FEC forward error correction code)	BER			$1x10^{-12}$		3
Maximum transmission distance						
OM3 multimode fiber	Lmax1			70	M	3
OM4 multimode fiber	Lmax2			100	M	3

Notes:
1.Support 100GBASE-SR4, IEEE803.3bm.
2.Tested using the pseudo-random code PBRS31.
3.Need to use forward error correction code FEC.

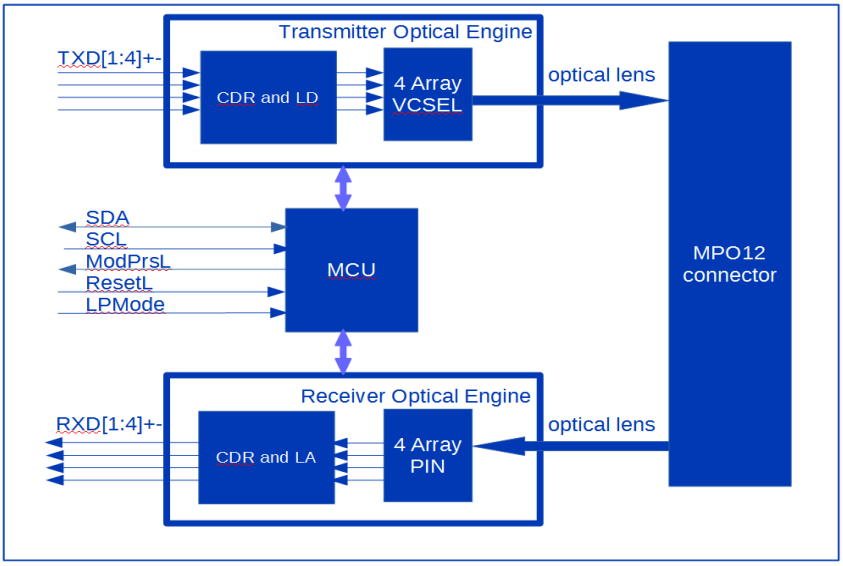
Electrical – Characteristics – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per lane	DR		25.78125		Gb/s	
Differential data input swing	V_{IN_PP}	180		1200	mV	
Transmit disable voltage	V_D	V_{CC}-1.3		V_{CC}	V	
Transmit enable voltage	V_{EN}	V_{EE}		V_{EE}+0.8	V	

Electrical – Characteristics – Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per lane	DR		25.78125		Gb/s	
Differential Data Output Swing	V_{OUT_PP}	400	600	800	mV	
Single Ended Voltage Tolerance	V	-0.35		3.3	V	
Data Output Rise/Fall Time (20%-80%)	t_r/t_f	12			ps	

Block-Diagram-of-Transceiver



Functions Description

MODULETEK's QSFP28-SR4-E10 module is manufactured using the advanced COB (Chip on Board) process. It consists of a microcontroller, a transmitter optical engine and a receiver optical engine. The module has built-in clock and data recovery functions. The default 4 channels are fixed at 25.78Gbps rate range. Modify the settings. The module can also work in the 28Gbps range and support OTN services.If you need other speed range versions or dual rate range versions, you can contact us for special customization.

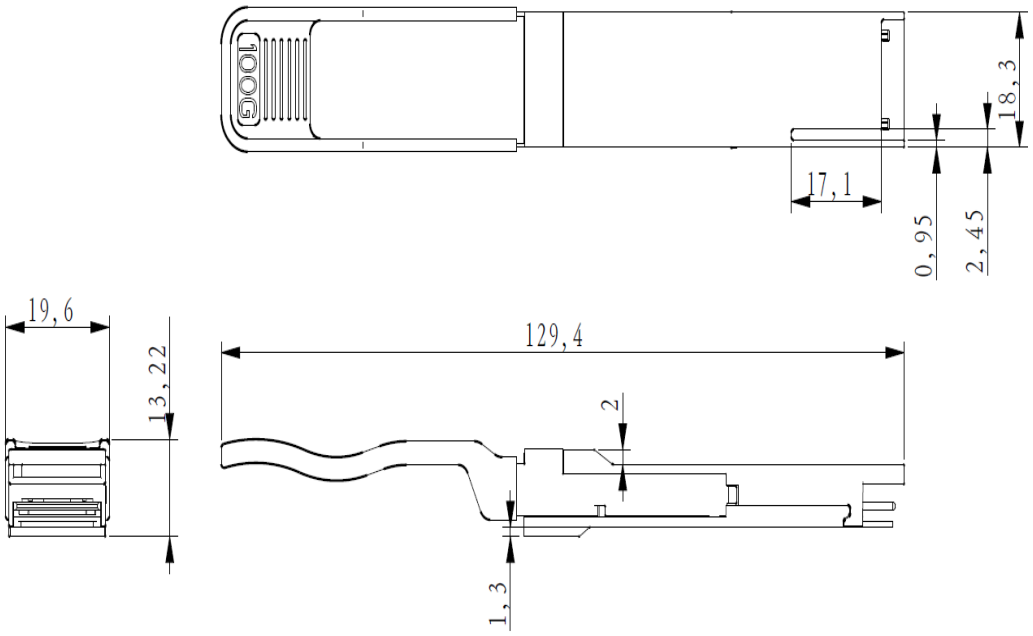
The transmitter optical engine includes a 4-channel transmitter clock data recovery (CDR) and laser driver circuit (LD), a 4-channel VCSEL laser array, and a 4-channel detection photodiode (MPD) array. The high-speed differential electrical signal output by the host is sent to the laser driver for amplification by CDR recovery shaping, driving the VCSEL laser to generate an optical signal, and the optical signal is coupled to the optical fiber through the optical lens. The light engine integrates a photodiode for detection for output optical power detection, and the laser driver uses an automatic optical power control loop to ensure the stability of the transmitted optical power.

The receiver optical engine includes a 4-channel photodiode (PIN) array, a 4-channel signal amplifier (TIA/LA) and a receiver-side clock data recovery circuit (CDR) array. The optical signal in the fiber is coupled to a receiving photodiode (PIN) through an optical lens to convert it into a photocurrent.T he photo-generated current signal is amplified by the amplifier, sent to the CDR circuit and recovered from the clock and data signals, and finally output to the host as a high-speed differential signal.

The microcontroller communicates with the host via a 2-wire serial communication interface, providing module control, status reporting and monitoring (DOM). This product complies with the SFF-8636 standard.

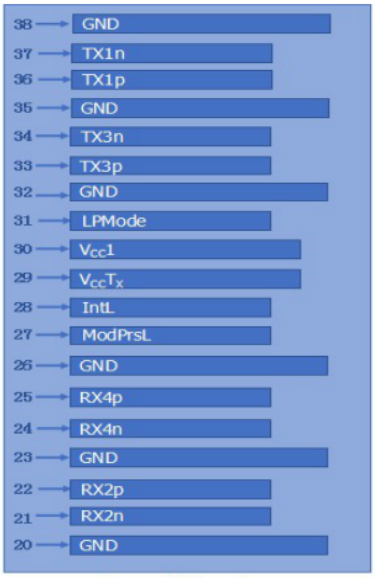
This product complies with the requirements of the IEEE 802.3bm standard. With the support of RS-FEC, it can reach a transmission distance of 100 meters in OM4 fiber.

Dimensions

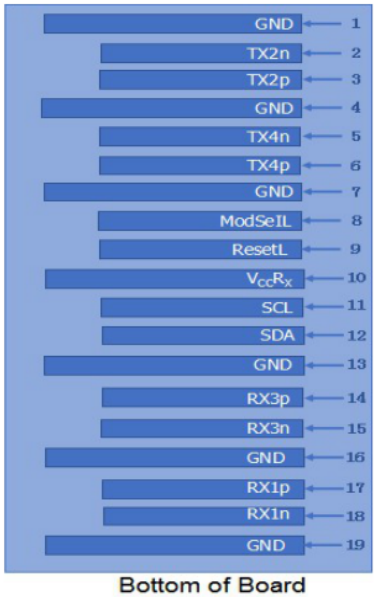


ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED
UNIT: mm

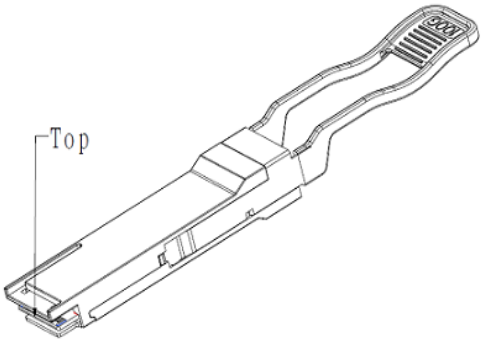
Electrical Pad Layout

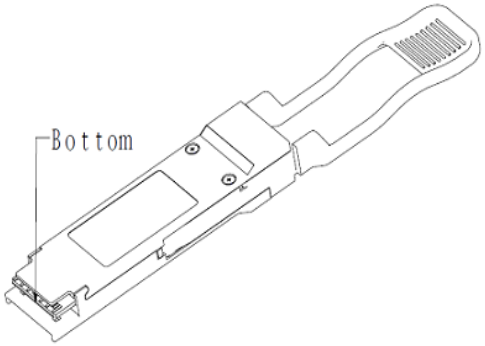


Top of Board



Bottom of Board





Pin Assignment

PIN #	Symbol	Description	Remarks
1	GND	Ground	5
2	Tx2n	Transmitter Inverted Data Input, LAN2	
3	Tx2p	Transmitter Non-Inverted Data Input, LAN2	
4	GND	Ground	5
5	Tx4n	Transmitter Inverted Data Input, LAN4	
6	Tx4p	Transmitter Non-Inverted Data Input, LAN4	
7	GND	Ground	5
8	ModSelL	Module select pin, the module responds to two-wire serial communication when low level	1
9	ResetL	Module Reset	2
10	$V_{cc}R_X$	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	5
14	Rx3p	Receiver Non-Inverted Data Output, LAN3	
15	Rx3n	Receiver Inverted Data Output, LAN3	
16	GND	Ground	5
17	Rx1p	Receiver Non-Inverted Data Output, LAN1	
18	Rx1n	Receiver Inverted Data Output, LAN1	
19	GND	Ground	5
20	GND	Ground	5
21	Rx2n	Receiver Inverted Data Output, LAN2	
22	Rx2p	Receiver Non-Inverted Data Output, LAN2	
23	GND	Ground	5
24	Rx4n	Receiver Inverted Data Output, LAN4	
25	Rx4p	Receiver Non-Inverted Data Output, LAN4	
26	GND	Ground	5
27	ModPrsL	The module is inserted into the indicate pin and grounded in the module.	3
28	IntL	Interrupt	4
29	$V_{cc}T_X$	+3.3V Power Supply transmitter	
30	V_{cc1}	+3.3V Power Supply	
31	LPMode	Low Power Mode	5
32	GND	Ground	5

33	Tx3p	Transmitter Non-Inverted Data Input, LAN3	
34	Tx3n	Transmitter Inverted Data Input, LAN3	
35	GND	Ground	5
36	Tx1p	Transmitter Non-Inverted Data Input, LAN1	
37	Tx1n	Transmitter Inverted Data Input, LAN1	
38	GND	Ground	5

Notes:
1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL is High, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module
2. The module restart pin, when the low level on the ResetL pin lasts longer than the minimum pulse length, resets the module and restores all user modules to their default state. When performing reset device, the host should ignore all status bits. Until the module reset interrupt is completed, please note that during hot plugging, the module will issue this information to complete the reset interrupt without resetting
3. This pin is active high, indicating that the module is running under a low power module.
4. IntL is the output pin, which is the open collector output and must be pulled up to Vcc on the motherboard. When it is low, it indicates that the module may malfunction. The host uses a 2-wire serial interface to identify the interrupt source
5.Circuit ground is internally isolated from chassis ground.

References

1. IEEE standard 802.3bm. IEEE Standard Department.
2. QSFP28 4X PLUGGABLE TRANSCEIVER –SFF-8665.
3. SFF-8636 Specification for Management Interface for Cabled Environments.