DATA SHEET

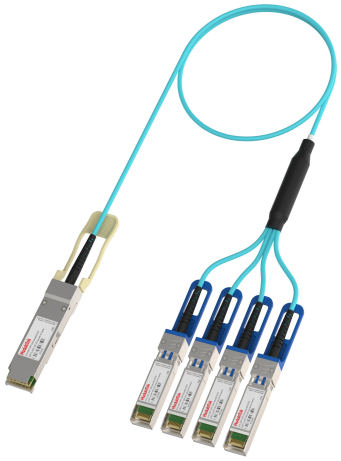
MODULETEK: AOC-QSFP-4SFP-100G-aaa.aaM-D1D1C

100G QSFP to 4xSFP Active Optical Cable Transceiver

Overview

AOC-QSFP-4SFP-100G-aaa.aaM-D1D1C QSFP to 4xSFP active optical cable transceiver is used to convert 100G QSFP to four 25G SFP branches, using full duplex optical components to 4 independent transmission and reception channels, each channel can support a transmission rate of 25.78 Gbps.

Product Features



- QSFP: Compliant with QSFP28 MSA
- SFP: Compliant with SFP+ MSA
- QSFP: 4 independent high-speed full duplex channels
- QSFP: Each channel bit rate at 25.78 Gbps
- Support Hot-pluggable
- 850 nm VCSEL laser transmitter
- PIN receiver
- Built-in digital diagnostic functions
- OM3 cable lengths up to 70 m
- OM4 cable lengths up to 100 m
- Single power supply 3.3 V
- RoHS compliant
- Low power consumption (QSFP ≤2.0 W @ Single-end, SFP ≤0.75 W @ Single-end)
- Operating temperature range (Case Temperature)：Commercial Level: 0 °C to 70 °C

Applications

- 100G Ethernet

Ordering Information

Part Number	Product ID	Description	Color on Clasp
AOC-QSFP-4SFP-100G-aaa.aaM-D1D1C	M365401	100G QSFP to 4xSFP active optical cable, available in lengths from 1 m to 100 m	Beige(QSFP), Blue(SFP)

Notes:
1. Product ID is the abbreviated order number of our company's product standard model
2. Model AOC-QSFP-4SFP-100G-aaa.aaM-D1D1C, where aaa.aa M refers to the length of the AOC cable

For more information or to order the above product, please contact:

Email: sales@moduletek.com

ModuleTek Website: www.moduletek.com

General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Line Rate (Per Channel)	BR		25.78		Gbps	
Bit Error Rate	BER			$5x10^{-5}$		1
Operating Temperature	T_C	0		70	°C	2
Storage Temperature	T_{STO}	-40		85	°C	3
Input Voltage	V_{CC}	3.13	3.3	3.46	V	
Maximum Voltage	V_{MAX}	-0.5		4	V	4

Notes:
1. Measured with line rate at 25.78 Gbps, PRBS 2^{31}-1
2. Case temperature
3. Ambient temperature
4. For electrical power interface

Electrical Characteristics – Transmitter

V_{CC} = 3.13 V to 3.46 V, T_C

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Input Differential Impedance (SFP)	R_{IN}		100		Ω	
Input Differential Impedance (QSFP)	R_{IN}		100		Ω	
Differential Data Input Swing (SFP)	V_{IN_PP}	180		1600	mV	
Differential Data Input Swing (QSFP)	V_{IN_PP}	180		1200	mV	
Transmitter Disable Voltage	V_D	2		V_{CC}	V	
Transmitter Enable Voltage	V_{EN}	V_{EE}		V_{EE}+0.8	V	

Electrical Characteristics – Receiver

V_{CC} = 3.13 V to 3.46 V, T_C

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Differential Date Output Swing (SFP)	V_{OUT_PP}	370	600	850	mV	
Differential Date Output Swing (QSFP)	V_{OUT_PP}	300	600	850	mV	
LOS Assert	V_{LOS_A}	2		V_{CC_HOST}	V	
LOS De-Assert	V_{LOS_D}	V_{EE}		V_{EE}+0.8	V	

Digital Diagnostic Function

AOC-QSFP-4SFP-100G-aaa.aaM-D1D1C supports the 2-wire serial communication protocol, QSFP defined in SFF-8636, and SFP defined in SFF-8472, which provides access to digital diagnostic information through a 2-wire interface. The internal microcontroller unit provides real-time access to module operating parameters such as module temperature, laser bias current, transmit optical power, receive optical power and module supply voltage. The QSFP module implements the alarm function of the SFF-8636, and SFP module implements the alarm function of the SFF-8472, which alerts the user when specific operating parameters are out of normal range.

QSFP Digital Diagnostic Threshold Range				
Parameter	**High Alarm**	**High Warning**	**Low Warning**	**Low Alarm**
Temperature (°C)	75.00 (4B00h)	70.00 (4600h)	0.00 (0000h)	-5.00 (FB00h)
Voltage (V)	3.63 (8DCCh)	3.46 (8728h)	3.13 (7A44h)	2.97 (7404h)
Bias Current (mA)	12.00 (1770h)	11.50 (1676h)	2.00 (03E8h)	1.00 (01F4h)
Tx Power (dBm)	3.40 (5575h)	2.40 (43E2h)	-8.40 (05A5h)	-9.40 (047Ch)
Rx Power (dBm)	3.40 (5575h)	2.40 (43E2h)	-10.30 (03A5h)	-11.30 (02E5h)

SFP Digital Diagnostic Threshold Range				
Parameter	**High Alarm**	**High Warning**	**Low Warning**	**Low Alarm**
Temperature (°C)	75.00 (4B00h)	70.00 (4600h)	0.00 (0000h)	-5.00 (FB00h)
Voltage (V)	3.63 (8DCCh)	3.46 (8728h)	3.13 (7A44h)	2.97 (7404h)
Bias Current (mA)	12.00 (1770h)	11.50 (1676h)	2.00 (03E8h)	1.00 (01F4h)
Tx Power (dBm)	3.40 (5575h)	2.40 (43E2h)	-8.40 (05A5h)	-9.40 (047Ch)
Rx Power (dBm)	3.40 (5575h)	2.40 (43E2h)	-10.30 (03A5h)	-11.30 (02E5h)

QSFP A0h Write Protection

Security Level 1 Password (Factory Value)		
Password Entry Bytes	**Size**	**Value (hex)**
A0h, 7Bh-7Eh	4	00 00 10 11

AOC-QSFP-4SFP-100G-aaa.aaM-D1D1C QSFP module has the function of A0h write-protection. Transceiver need enter the security level 1 working state to write the contents of page 00h and page 02h of the device address A0h. The method to enter the security level 1 working state is to write the security level 1 password sequentially in the 7Bh-7Eh bytes of the device address A0h. After entering the security level 1, the user can modify the contents of the 7Fh page select byte of the device address A0h to write the contents of page 00h and page 02h. This version of the module supports users to modify the level 1 security password. To do so, the user must first enter security level 1, then write the new level 1 password into the registers 77h-7Ah (Password change entry) at device address A0h. The valid range for the new level 1 password is 00000000-7FFFFFFF (hex), and the most significant bit of the new password must be 0b.

SFP A0h/A2h Write Protection

Security Level 1 Password (Factory Value)		
Password Entry Bytes	**Size**	**Value (hex)**
A2h, 7Bh-7Eh	4	00 00 10 11
Change Security Level 1 Password		
Change Password Entry Bytes	**Size**	**Value (hex)**
A2h, Page F0h, 80h-83h	4	Programmed by User

AOC-QSFP-4SFP-100G-aaa.aaM-D1D1C SFP module has the function of A0h and A2h write protection. Transceiver need enter the security level 1 working state to write the device address A0h as well as page 00h, page 01h and page F0h of device address A2h. The method to enter the security level 1 working state is to write the security level 1 password sequentially to bytes 7Bh-7Eh of the device address A2h. After entering the security level 1, the user can either write directly to device address A0h or write to page 00h, page 01h and page F0h of device address A2h by modifying 7Fh page select byte of the device address A2h. This version module supports users to modify the password of security level 1 by writing a new security level 1 password in the 80h-83h register in the device address F0h page of module A2h. The new security level 1 password ranges from 00000000-7FFFFFFF (hex), and the highest bit of the new security level 1 password must be 0b.

QSFP A0h Memory Map Low 128 Bytes

Lower Memory Map (A0h)				
Byte	**Size**	**Name**	**Description**	**Initial Value (hex)**
0	1	Identifier	QSFP28	11
1	1	Revision Compliance	SFF-8636 Rev 2.10	08
2	1	Status	Bit7:3 = 00000: Reserved Bit2 = 0: Upper memory paged Bit1: Digital state of the IntL interrupt output pin Bit0: Data_Not_Ready	Variable
3	1	Channel Status LOS Flag	Tx/Rx LOS flag	Variable
4	1	Channel Status TX Adapt EQ Fault/Tx_Fault Flag	Bit7:4: This product does not support TX adapt EQ fault flag Bit3:0: Tx_Fault flag	Variable

5	1	Channel Status LOL Flag	Tx/Rx CDR LOL flag	Variable
6	1	Module Monitor Temperature Alarm/Warning Flag	Bit7:4: Temperature alarm/warning flag Bit3:2: Reserved Bit1: This product does not support TC readiness flag Bit0: initialization completion flag bit	Variable
7	1	Module Monitor Vcc Alarm/Warning Flag	Vcc alarm/warning flag	Variable
8	1	Vendor Specific	Vendor specific information	00
9-10	2	Channel Monitor Rx Power Alarm/Warning Flag	Rx power alarm/warning flag	Variable
11-12	2	Channel Monitor Tx Bias Alarm/Warning Flag	Tx bias alarm/warning flag	Variable
13-14	2	Channel Monitor Tx Power Alarm/Warning Flag	Tx power alarm/warning flag	Variable
15-18	4	Reserved	Reserved channel monitor flags	00 00 00 00
19-21	3	Vendor Specific	Vendor specific information	00 00 00
22-23	2	Module Monitor Temperature	Temperature diagnosis, unit is 1/256 °C	Variable
24-25	2	Reserved	Reserved	00 00
26-27	2	Module Monitor Voltage	Supply voltage diagnosis, unit is 100 uV	Variable
28-29	2	Reserved	Reserved	00 00
30-33	4	Vendor Specific	Vendor specific information	00 00 00 00
34-35	2	Channel Monitor Rx1 Power	Rx1 average receive power diagnosis, unit of 0.1 uW	Variable
36-37	2	Channel Monitor Rx2 Power	Rx2 average receive power diagnosis, unit of 0.1 uW	Variable
38-39	2	Channel Monitor Rx3 Power	Rx3 average receive power diagnosis, unit of 0.1 uW	Variable

40-41	2	Channel Monitor Rx4 Power	Rx4 average receive power diagnosis, unit of 0.1 uW	Variable
42-43	2	Channel Monitor Tx1 Bias	Tx1 bias current diagnosis, unit of 2 uA	Variable
44-45	2	Channel Monitor Tx2 Bias	Tx2 bias current diagnosis, unit of 2 uA	Variable
46-47	2	Channel Monitor Tx3 Bias	Tx3 bias current diagnosis, unit of 2 uA	Variable
48-49	2	Channel Monitor Tx4 Bias	Tx4 bias current diagnosis, unit of 2 uA	Variable
50-51	2	Channel Monitor Tx1 Power	Tx1 average optical power diagnosis, unit of 0.1 uW	Variable
52-53	2	Channel Monitor Tx2 Power	Tx2 average optical power diagnosis, unit of 0.1 uW	Variable
54-55	2	Channel Monitor Tx3 Power	Tx3 average optical power diagnosis, unit of 0.1 uW	Variable
56-57	2	Channel Monitor Tx4 Power	Tx4 average optical power diagnosis, unit of 0.1 uW	Variable
58-73	16	Reserved	Reserved	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
74-81	8	Vendor Specific	Vendor specific information	00 00 00 00 00 00 00 00
82-85	4	Reserved	Reserved	00 00 00 00
86	1	Control TxDisable	Bit7:4 = 0000: Reserved Bit3: Bit of channel4 laser disable control Bit2: Bit of channel3 laser disable control Bit1: Bit of channel2 laser disable control Bit0: Bit of channel1 laser disable control	00
87	1	Control Rx Rate Select	This product does not support this function, initialize to 00h	00
88	1	Control Tx Rate Select	This product does not support this function, initialize to 00h	00
89-92	4	Reserved	Reserved	00 00 00 00

93	1	Control Power	Bit7 = 0: Software reset implemented Bit6:4 = 000: Reserved Bit3 = 0: Default 0, high power class(Class 8) implemented Bit2 = 0: Default 0, high power class(Class 5-7) implemented Bit1 = 0: Default 0, Low power mode(Class 1) implemented Bit0 = 0: Default 0, Software power management enable	00
94-97	4	Reserved	Reserved	00 00 00 00
98	1	Control Tx/Rx CDR	Bit7 = 1: Channel4 Tx CDR on Bit6 = 1: Channel3 Tx CDR on Bit5 = 1: Channel2 Tx CDR on Bit4 = 1: Channel1 Tx CDR on Bit3 = 1: Channel4 Rx CDR on Bit2 = 1: Channel3 Rx CDR on Bit1 = 1: Channel2 Rx CDR on Bit0 = 1: Channel1 Rx CDR on	FF
99	1	Control LP/TxDis, IntL/LOSL	Bit7:2 = 000000: Reserved Bit1: LPMode/TxDis input signal control Bit0: IntL/LOSL output signal control	00
100	1	Mask Tx/Rx LOS	Masking Tx/Rx LOS	00
101	1	Mask Tx Adapt EQ Fault/Tx Fault	Bit7:4: This product does not support mask Tx adapt EQ fault Bit3:0: Masking Tx fault	00
102	1	Mask Tx/Rx CDR LOL	Masking Tx/Rx CDR LOL	00
103	1	Mask Temperature Alarm/Warning	Masking temperature alarm/warning	00
104	1	Mask Vcc Alarm/Warning	Masking voltage alarm/warning	00
105-106	2	Vendor Specific	Vendor specific information	00 00
107	1	Max Power Consumption	Maximum power consumption of module 2.0 W, unit of 0.1 W	14
108-109	2	Propagation Delay	This product does not support this function, initialize to 00h	00 00
110	1	Free Side Device Properties	Bit7:4 = 0000: Power 1.5 W or higher Bit3 = 0: The far end is managed and complies with SFF-8472 Bit2:0 = 000: 3.3 V	00
111-112	2	Assigned for use by PCI Express	This product does not support this function, initialize to 00h	00 00

113	1	Free Side Device Properties	Bit7 = 0: Reserved Bit6:4 = 100: 4 far-ends with 1 channel implemented in each Bit3:0 = 0000: Near-End implementation	40
114	1	Use by microQSFP	This product does not support this function, initialize to 00h	00
115	1	ModSelL wait time	This product does not support this function, initialize to 00h	00
116	1	Secondary Extended Spec Compliance	100G Base AOC. Providing a worst BER of 5×10^{-5}	01
117-118	2	Reserved	Reserved	00 00
119-122	4	Password Change Entry Area (optional)	Modify security level 1 password entry, power-up default 00000000 (hex); readback not supported after writing	00 00 00 00
123-126	4	Password Entry Area (optional)	Security level 1 password entry, power-up default 00000000 (hex); readback not supported after writing	00 00 00 00
127	1	Page Select Byte	Page selection, select A0h high 128 bytes page	00

QSFP A0h Memory Map High 128 Bytes

Upper Memory Map Page 00h				
Byte	**Size**	**Name**	**Description**	**Initial Value (hex)**
128	1	Identifier	QSFP28	11
129	1	Ext. Identifier	Bit7:6 = 01: Power Class 2 module (≤2.0 W) Bit5 = 0: Power Class 8 not implemented Bit4 = 0: No CLEI code Bit3 = 1: Tx with CDR function Bit2 = 1: Rx with CDR function Bit1:0 = 00: Power Classes 1 to 4	4C
130	1	Connector Type	No separable connector	23
131-138	8	Specification Compliance	100G Base AOC. Providing a worst BER of 5×10^{-5}	80 00 00 00 00 00 00 00
139	1	Encoding	NRZ	03
140	1	Nominal bit rate	Unit is 100 Mbps	FF
141	1	Extended Rate Select Compliance	No rate selection function	00

142	1	Length (SMF)	SMF transmission distance, unit of 1 km	00
143	1	Length (OM3 50 um)	OM3 transmission distance, unit of 2 m	00
144	1	Length (OM2 50 um)	OM2 transmission distance, unit of 1 m	00
145	1	Length (OM1 62.5 um)	OM1 transmission distance, unit of 1 m	00
146	1	Length(Active Cable or Copper)	Cable length, unit of 1 m	According to customer needs
147	1	Device technology	Bit7:4 = 0000: 850 nm VCSEL Bit3 = 0: No wavelength control Bit2 = 0: Uncooled transmitter device Bit1 = 0: Pin detector Bit0 = 0: Transmitter not tunable	00
148-163	16	Vendor name	MODULETEK	4D 4F 44 55 4C 45 54 45 4B 20 20 20 20 20 20 20
164	1	Extended Module	InfiniBand applications are not supported	00
165-167	3	Vendor OUI	IEEE company identifier for the vendor	00 00 00
168-183	16	Vendor PN	Vendor Part Number	ASCII Format
184-185	2	Vendor rev	Vendor Part Revision Number	Defined by vendor
186-187	2	Wavelength	Undefined	00 00
188-189	2	Wavelength tolerance	Undefined	00 00
190	1	Max case temp	Max case temp is 70 °C, unit of °C	46
191	1	CC_BASE	Check sum of bytes 128-190	Defined by vendor
192	1	Extended Specification Compliance Codes	100G Base AOC. Providing a worst BER of 5×10^{-5}	01

193	1	Options	Bit7 = 0: Reserved Bit6 = 1: LPMode/TxDis input signal is configurable using byte 99, bit 1 Bit5 = 1: IntL/RxLOSL output signal is configurable using byte 99, bit 0 Bit4 = 0: Tx input adaptive equalizers freeze capable not implemented Bit3 = 0: Tx input equalizers auto-adaptive capable not implemented Bit2 = 1: Tx input equalizers fixed-programmable implemented Bit1 = 1: Rx output emphasis fixed-programmable implemented Bit0 = 1: Rx output amplitude fixed-programmable implemented	67
194	1	Options	Bit7 = 1: Tx CDR On/Off control implemented Bit6 = 1: Rx CDR On/Off control implemented Bit5 = 1: Tx CDR loss of lock (LOL) flag implemented Bit4 = 1: Rx CDR loss of lock (LOL) flag implemented Bit3 = 1: Rx squelch disable implemented Bit2 = 1: Rx output disable capable implemented Bit1 = 1: Tx squelch disable implemented Bit0 = 1: Tx squelch implemented	FF
195	1	Options	Bit7 = 1: Memory page 02h provided Bit6 = 0: Memory page 01h not provided Bit5 = 0: Rate selection function not implemented Bit4 = 1: Tx_DISABLE implemented Bit3 = 1: Tx_FAULT signal implemented Bit2 = 0: Tx squelch implemented to reducing by OMA Bit1 = 1: Tx los of signal implemented Bit0 = 0: Pages 20-21h not implemented	9A
196-211	16	Vendor SN	Vendor part serial number	Defined by vendor
212-219	8	Date Code	Date	Defined by vendor
220	1	Diagnostic Monitoring Type	Bit7:6 = 00: Reserved Bit5 = 1: Temperature monitoring implemented Bit4 = 1: Supply voltage monitoring implemented Bit3 = 1: Received power measurements type is average power Bit2 = 1: Transmitter power measurement supported Bit1:0 = 00: Reserved	3C

221	1	Enhanced Options	Bit7:5 = 000: Reserved Bit4 = 1: The initialization complete flag at byte 6 bit 0 is implemented Bit3 = 0: Does not support rate selection Bit2 = 0: This bit is reserved and reads 0 Bit1 = 0: TC readiness flag not implemented Bit0 = 1: Software reset is implemented. Use byte 93, bit 7	11
222	1	BR, nominal	Nominal baud rate, unit of 250 Mbps	68
223	1	CC_EXT	Check sum of bytes 192-222	Defined by vendor
224-255	32	Vendor Specific	Vendor specific information	Defined by vendor
Upper Memory Map Page 02h				
Byte	**Size**	**Name**	**Description**	**Initial Value (hex)**
128-255	128	User-writable EEPROM	User defined, readable and writeable under security level 1	User-defined
Upper Memory Map Page 03h				
Byte	**Size**	**Name**	**Description**	**Initial Value (hex)**
128-129	2	Temp High Alarm	Temperature high alarm	See Table of Threshold Ranges
130-131	2	Temp Low Alarm	Temperature low alarm	See Table of Threshold Ranges
132-133	2	Temp High Warning	Temperature high warning	See Table of Threshold Ranges
134-135	2	Temp Low Warning	Temperature low warning	See Table of Threshold Ranges
136-143	8	Reserved	Reserved	00 00 00 00 00 00 00 00
144-145	2	Vcc High Alarm	Voltage high alarm	See Table of Threshold Ranges

146-147	2	Vcc Low Alarm	Voltage low alarm	See Table of Threshold Ranges
148-149	2	Vcc High Warning	Voltage high warning	See Table of Threshold Ranges
150-151	2	Vcc Low Warning	Voltage low warning	See Table of Threshold Ranges
152-159	8	Reserved	Reserved	00 00 00 00 00 00 00 00
160-175	16	Vendor Specific	Vendor specific information	Defined by vendor
176-177	2	Rx Power High Alarm	Rx power high alarm	See Table of Threshold Ranges
178-179	2	Rx Power Low Alarm	Rx power low alarm	See Table of Threshold Ranges
180-181	2	Rx Power High Warning	Rx power high warning	See Table of Threshold Ranges
182-183	2	Rx Power Low Warning	Rx power low warning	See Table of Threshold Ranges
184-185	2	Tx Bias High Alarm	Tx bias current high alarm	See Table of Threshold Ranges
186-187	2	Tx Bias Low Alarm	Tx bias current low alarm	See Table of Threshold Ranges
188-189	2	Tx Bias High Warning	Tx bias current high warning	See Table of Threshold Ranges
190-191	2	Tx Bias Low Warning	Tx bias current low warning	See Table of Threshold Ranges

192-193	2	Tx Power High Alarm	Tx power high alarm	See Table of Threshold Ranges
194-195	2	Tx Power Low Alarm	Tx power low alarm	See Table of Threshold Ranges
196-197	2	Tx Power High Warning	Tx power high warning	See Table of Threshold Ranges
198-199	2	Tx Power Low Warning	Tx power low warning	See Table of Threshold Ranges
200-207	8	Reserved	Reserved	00 00 00 00 00 00 00 00
208-215	8	Reserved	Reserved	00 00 00 00 00 00 00 00
216-223	8	Vendor Specific	Vendor specific information	Defined by vendor
224	1	Tx EQ, Rx Emphasis Magnitude ID	Bit7:4 = 1010: Max Tx input equalization supported Bit3:0 = 0111: Max Rx output emphasis supported	A7
225	1	Rx output amplitude support indicators	Bit7:6 = 00: Reserved Bit5:4 = 00: Peak-to-peak amplitude stays constant Bit3:0 = 1111: Rx output amplitude supported	0F
226	1	Control options advertising	Reserved	00
227	1	Control options advertising	Bit7 = 0: This product does not support controllable host-side FEC Bit6 = 0: This product does not support controllable media-side FEC support Bit5:4 = 00: Reserved Bit3 = 1: Tx force squelch implemented Bit2 = 0: RxLOSL fast mode is not supported Bit1 = 1: Complies with timing requirements of SFF-8679 optional TxDis fast mode Bit0 = 0: Reserved	0A
228	1	Control options advertising	This product does not support maximum TC stabilization time, initialize to 00h	00

229	1	Control options advertising	This product does not support maximum CTLE settling time, initialize to 00h	00
230	1	Optional Channel Controls	Bit7 = 0: This product does not support host-side FEC Bit6 = 0: This product does not support media-side FEC Bit5:0 = 000000: Reserved	00
231	1	Optional Channel Controls	Bit7:4 = 0000: Reserved Bit3 = 0: Tx4 force squelch Bit2 = 0: Tx3 force squelch Bit1 = 0: Tx2 force squelch Bit0 = 0: Tx1 force squelch	00
232	1	Optional Channel Controls	Reserved	00
233	1	Optional Channel Controls	This product does not support controls to freeze Tx input adaptive equalizers, initialize to 00h	00
234	1	Optional Channel Controls	Bit7:4 = 0100: Tx1 input equalizer control Bit3:0 = 0100: Tx2 input equalizer control	44
235	1	Optional Channel Controls	Bit7:4 = 0100: Tx3 input equalizer control Bit3:0 = 0100: Tx4 input equalizer control	44
236	1	Optional Channel Controls	Bit7:4 = 0010: Rx1 output emphasis control Bit3:0 = 0010: Rx2 output emphasis control	22
237	1	Optional Channel Controls	Bit7:4 = 0010: Rx3 output emphasis control Bit3:0 = 0010: Rx4 output emphasis control	22
238	1	Optional Channel Controls	Bit7:4 = 0001: Rx1 output amplitude Bit3:0 = 0001: Rx2 output amplitude	11
239	1	Optional Channel Controls	Bit7:4 = 0001: Rx3 output amplitude Bit3:0 = 0001: Rx4 output amplitude	11
240	1	Optional Channel Controls	Bit7:4 = 0000: Rx4-Rx1 squelch enable Bit3:0 = 0000: Tx4-Tx1 squelch enable	00
241	1	Optional Channel Controls	Bit7:4 = 0000: Rx4-Rx1 output enable Bit3:0 = 0000: Tx4-Tx1 input adaptive equalizers disable	00
242-243	2	Channel Monitor Masks	Masking bit for Rx power alarm/warning	00 00

244-245	2	Channel Monitor Masks	Masking bit for Tx bias current alarm/warning	00 00
246-247	2	Channel Monitor Masks	Masking bit for Tx power alarm/warning	00 00
248-249	2	Channel Monitor Masks	Reserved	00 00
250-251	2	Channel Monitor Masks	Reserved	00 00
252-255	4	Reserved	Reserved	00 00 00 00

SFP A0h Memory Map

Byte	Size	Name	Description	Initial Value (hex)
0	1	Identifier	SFP	03
1	1	Extended Identifier	Two-wire interface	04
2	1	Connector	No separable connector	23
3-10	8	Transceiver	25G Base AOC	00 00 00 00 00 08 00 00
11	1	Encoding	Not explicitly specified	00
12	1	BR, Nominal	Nominal bit rate 25.78 Gb/s	FF
13	1	Rate Identifier	No rate selection function	00
14	1	Length (9 μm)-km	9 μm SMF link length = N/A	00
15	1	Length (9 μm)-100 m	9 μm SMF link length = N/A	00
16	1	Length (50 μm, OM2)-10 m	50 μm OM2 MMF link length = N/A	00
17	1	Length (62.5 μm, OM1)-10 m	62.5 μm OM1 MMF link length = N/A	00
18	1	Length (Active Cable)-m	Cable length-m	According to customer needs
19	1	Length (Active Cable)-m	Cable length-m	00

20-35	16	Vendor name	MODULETEK	4D 4F 44 55 4C 45 54 45 4B 20 20 20 20 20 20 20
36	1	Transceiver	25G Base AOC	01
37-39	3	Vendor OUI	Without vendor OUI	00 00 00
40-55	16	Vendor PN	Part number provided by SFP vendor	ASCII Format
56-59	4	Vendor Revision	Revision level for part number provided by vendor	Defined by vendor
60-61	2	Wavelength	Unallocated	00 00
62	1	Reserved	Unallocated	00
63	1	CC_BASE	Check sum of bytes 0-62	Defined by vendor
64	1	Transceiver Options	Bit7:6 = 00: Reserved Bit5 = 0: Power level 1, < 1.0 W Bit4 = 1: Paging function is implemented Bit3 = 1: With retimer or CDR indicator Bit2 = 0: Uncooled laser transmitter Bit1 = 0: Power level 1, < 1.0 W Bit0 = 0: Receiver output is conventional limiting	18
65	1	Transceiver Options	Bit7 = 0: Receiver decision threshold is not implemented Bit6 = 0: The transmitter wavelength is not tunable Bit5 = 0: RATE_SELECT functionality is not implemented Bit4 = 1: Tx_Disable is implemented Bit3 = 1: Tx_Fault is implemented Bit2 = 0: Signal detect is not implemented Bit1 = 1: Rx_LOS is implemented Bit0 = 0: Reserved	1A
66	1	BR, nominal	BR, nominal	67
67	1	BR, deviation	BR, deviation	00
68-83	16	Vendor SN	Manufacturer serial number	Defined by vendor
84-91	8	Date code	Date	Defined by vendor

92	1	Monitoring Type	Bit7 = 0: Compatible with SFF-8472 requirements Bit6 = 1: Digital diagnostic function is implemented Bit5 = 1: Internal calibration is implemented Bit4 = 0: Externally calibration is not implemented Bit3 = 1: Received power measurement type is average power Bit2 = 0: No address change required Bit1:0 = 00: Reserved	68
93	1	Enhanced Options	Bit7 = 1: Optional Alarm/Warning flags are implemented for all monitored quantities Bit6 = 1: Optional soft Tx_Disable control and monitoring are implemented Bit5 = 1: Optional soft Tx_Fault monitoring is implemented Bit4 = 1: Optional soft Rx_LOS monitoring is implemented Bit3 = 0: Optional soft RATE_SELECT control and monitoring are not implemented Bit2 = 0: Optional application select control is not implemented per SFF-8079 Bit1 = 0: Optional soft rate select control is not implemented per SFF-8431 Bit0 = 0: Reserved	F0
94	1	Compliance	Includes functionality described in Rev 12.3 of SFF-8472	08
95	1	CC_EXT	Check sum of bytes 64-94	Defined by vendor
96-127	32	Vendor Specific	Vendor specific memory addresses	Defined by vendor
128-255	128	Vendor Specific	Vendor specific memory addresses	Defined by vendor

SFP A2h Memory Map

Byte	Size	Name	Description	Initial Value (hex)
Lower Memory Map(A2h)				

00-01	2	Temp High Alarm	Temperature high alarm threshold	See Table of Threshold Ranges
02-03	2	Temp Low Alarm	Temperature low alarm threshold	See Table of Threshold Ranges
04-05	2	Temp High Warning	Temperature high warning threshold	See Table of Threshold Ranges
06-07	2	Temp Low Warning	Temperature low warning threshold	See Table of Threshold Ranges
08-09	2	Voltage High Alarm	Voltage high alarm threshold	See Table of Threshold Ranges
10-11	2	Voltage Low Alarm	Voltage low alarm threshold	See Table of Threshold Ranges
12-13	2	Voltage High Warning	Voltage high warning threshold	See Table of Threshold Ranges
14-15	2	Voltage Low Warning	Voltage low warning threshold	See Table of Threshold Ranges
16-17	2	Bias High Alarm	Bias current high alarm threshold	See Table of Threshold Ranges
18-19	2	Bias Low Alarm	Bias current low alarm threshold	See Table of Threshold Ranges
20-21	2	Bias High Warning	Bias current high warning threshold	See Table of Threshold Ranges
22-23	2	Bias Low Warning	Bias current low warning threshold	See Table of Threshold Ranges

24-25	2	TX Power High Alarm	TX power high alarm threshold	See Table of Threshold Ranges
26-27	2	TX Power Low Alarm	TX power low alarm threshold	See Table of Threshold Ranges
28-29	2	TX Power High Warning	TX power high warning threshold	See Table of Threshold Ranges
30-31	2	TX Power Low Warning	TX power low warning threshold	See Table of Threshold Ranges
32-33	2	RX Power High Alarm	RX power high alarm threshold	See Table of Threshold Ranges
34-35	2	RX Power Low Alarm	RX power low alarm threshold	See Table of Threshold Ranges
36-37	2	RX Power High Warning	RX power high warning threshold	See Table of Threshold Ranges
38-39	2	RX Power Low Warning	RX power low warning threshold	See Table of Threshold Ranges
40-41	2	Optional Laser Temp High Alarm	This function is not implemented	00 00
42-43	2	Optional Laser Temp Low Alarm	This function is not implemented	00 00
44-45	2	Optional Laser Temp High Warning	This function is not implemented	00 00
46-47	2	Optional Laser Temp Low Warning	This function is not implemented	00 00
48-49	2	Optional TEC Current High Alarm	This function is not implemented	00 00

50-51	2	Optional TEC Current Low Alarm	This function is not implemented	00 00
52-53	2	Optional TEC Current High Warning	This function is not implemented	00 00
54-55	2	Optional TEC Current Low Warning	This function is not implemented	00 00
56-59	4	RX_PWR(4)	External calibration data for RX optical power, the module only implements an internally calibrated function	00 00 00 00
60-63	4	RX_PWR(3)	External calibration data for RX optical power, the module only implements an internally calibrated function	00 00 00 00
64-67	4	RX_PWR(2)	External calibration data for RX optical power, the module only implements an internally calibrated function	00 00 00 00
68-71	4	RX_PWR(1)	External calibration data for RX optical power, the module only implements an internally calibrated function	3F 80 00 00
72-75	4	RX_PWR(0)	External calibration data for RX optical power, the module only implements an internally calibrated function	00 00 00 00
76-77	2	TX_I(Slope)	External calibration data for laser bias current, the module only implements an internally calibrated function	01 00
78-79	2	TX_I(Offset)	External calibration data for laser bias current, the module only implements an internally calibrated function	00 00
80-81	2	TX_PWR(Slope)	External calibration data for TX optical power, the module only implements an internally calibrated function	01 00
82-83	2	TX_PWR(Offset)	External calibration data for TX optical power, the module only implements an internally calibrated function	00 00
84-85	2	T(Slope)	External calibration data for internal module temperature, the module only implements an internally calibrated function	01 00
86-87	2	T(Offset)	External calibration data for internal module temperature, the module only implements an internally calibrated function	00 00

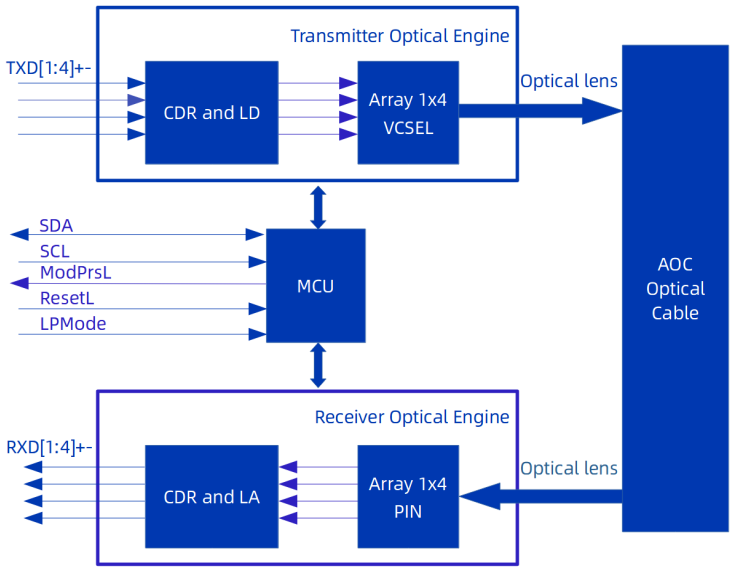
88-89	2	V(Slope)	External calibration data for internal module supply voltage, the module only implements an internally calibrated function	01 00
90-91	2	V(Offset)	External calibration data for internal module supply voltage, the module only implements an internally calibrated function	00 00
92-94	3	Reserved	Reserved	00 00 00
95	1	Checksum	Check sum of bytes 0-94	Defined by vendor
96-97	2	Temperature	Internally measured module temperature, unit is 1/256 °C	Variable
98-99	2	Vcc	Internally measured supply voltage in module, unit is 100 uV	Variable
100-101	2	TX Bias	Internally measured TX bias current, unit is 2 uA	Variable
102-103	2	TX Power	Internally measured TX output power, unit is 0.1 uW	Variable
104-105	2	RX Power	Internally measured RX input power, unit is 0.1 uW	Variable
106-107	2	Optional Laser Temp	This function is not implemented	00 00
108-109	2	Optional TEC current	This function is not implemented	00 00
110	1	Status/Control	Bit7: Tx_Disable input pin state Bit6 = 0: Laser disable control bit. Writing '1' disables laser Bit5: RS1 pin state Bit4: RS0 pin state Bit3 = 0: Soft RS0 control bit. Soft rate select is not implemented Bit2: Tx_Fault pin state Bit1: Rx_LOS pin state Bit0: Data_Ready_Bar state. Zero/low indicates that the module data is ready	Variable
111	1	Reserved	Reserved for SFF-8079	00
112	1	Alarm Flags	Bit7: Temp high alarm flag, active high Bit6: Temp low alarm flag, active high Bit5: Vcc high alarm flag, active high Bit4: Vcc low alarm flag, active high Bit3: TX bias high alarm flag, active high Bit2: TX bias low alarm flag, active high Bit1: TX power high alarm flag, active high Bit0: TX power low alarm, active high	Variable

113	1	Alarm Flags	Bit7: RX power high alarm flag, active high Bit6: RX power Low alarm flag, active high Bit5: Optional laser temp high alarm flag, this alarm flag is not implemented Bit4: Optional laser temp Low alarm flag, this alarm flag is not implemented Bit3: Optional TEC current high alarm flag, this alarm flag is not implemented Bit2: Optional TEC current low alarm flag, this alar m flag is not implemented Bit1:0: Reserved alarm flag	Variable
114	1	Tx input equalization control	Bit7:4 = 0011: High-speed mode input equalization setting value; the default value for power-up is 3, which can be used to change the module input equalization value Bit3:0 = 0011: Low-speed mode input equalization setting value; not used, the default value for power-up is 3	33
115	1	Rx out emphasis Control	Bit7:4 = 0011: High-speed mode output emphasis setting value; the default value for power-up is 3, which can be used to change the module output emphasis value Bit3:0 = 0011: Low-speed mode output emphasis setting value; not used, the default value for power-up is 3	33
116	1	Warning Flags	Bit7: Temp high warning flag, active high Bit6: Temp low warning flag, active high Bit5: Vcc high warning flag, active high Bit4: Vcc low warning flag, active high Bit3: TX Bias high warning flag, active high Bit2: TX bias low warning flag, active high Bit1: TX power high warning flag, active high Bit0: TX power low warning flag, active high	Variable

117	1	Warning Flags	Bit7: RX power high warning flag, active high Bit6: RX power low warning flag, active high Bit5: Optional laser temp high warning flag, this warning flag is not implemented Bit4: Optional laser temp low warning flag, this warning flag is not implemented Bit3: Optional TEC current high warning flag, this warning flag is not implemented Bit2: Optional TEC current low warning flag, this warning flag is not implemented Bit1:0: Reserved warning flag	Variable
118	1	Ext Status/Control	Bit7:4 = 0: Reserved Bit3 = 0: Soft RS1 control bit. Soft rate select is not implemented Bit2 = 0: Reserved Bit1 = 0: Power level state = Level 1, < 1.0 W Bit0 = 0: Power level select = Level 1, < 1.0 W	00
119	1	Ext Status/Control	Bit7:5 = 0: Reserved Bit4 = 0: 64GFC Mode Tx configured, this function is not implemented Bit3 = 0: 64GFC Mode Rx configured, this function is not implemented Bit2 = 0: 64GFC Mode configured, this function is not implemented Bit1: TX CDR state, 0 = CDR is locked, 1 = CDR loss of lock Bit0: RX CDR state, 0 = CDR is locked, 1 = CDR loss of lock	Variable
120-122	3	Reserved	Reserved	00 00 00
123-126	4	Security Level Password	Security level password entry. The written value can be read back and the default value on power-up is 00 00 00 00(hex)	00 00 00 00
127	1	Page selection byte	Page selection, select A2h high 128 bytes page	00
Upper Memory Map Page 00/01h				
128-255	128	User Writable EEPROM	User defined, readable and writeable under security level 1	Defined by vendor

Notes:
1. The alarm threshold information can be modified according to the customer's definition, please contact us if you have any modification requirements

QSFP Block Diagram of Transceiver



QSFP Functions Description

AOC-QSFP-4SFP-100G-aaa.aaM-D1D1C QSFP module is manufactured by COB (Chip on Board) process and consists of a microcontroller, a transmitter side optical engine and a receiver side optical engine. The module has built-in clock and data recovery functions, and the operating rate of the built-in CDR at the transmitter and receiver is: 25.5 Gbps-26 Gbps. If you need another version of the rate range, you can contact us for special customization.

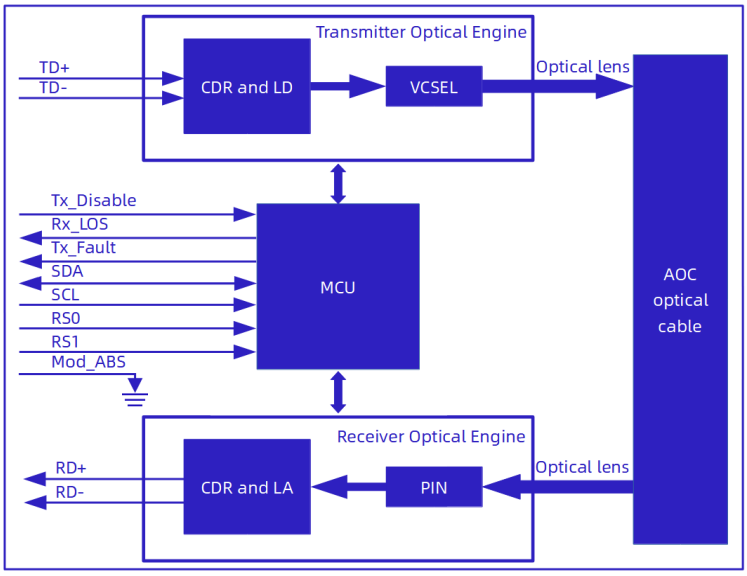
The microcontroller communicates with the host via a 2-wire serial communication interface and provides module control, status reporting, and monitoring (DOM) functions in accordance with the SFF-8636 standard.

The transmitter side optical engine consists of a 4-channel clock data recovery circuit (CDR) and 4-channel laser driver circuit (LD), a 4-channel VCSEL laser array. The high-speed differential electrical signals output from the host is restored and shaped by the CDR. The restored electrical signal send to the laser driver and drive the VCSEL lasers to generate optical signals. The optical signals are coupled into the optical fiber through an optical lens.

The receiver side optical engine consists of a 4-channel clock data recovery circuit (CDR) and 4-channel signal amplifier (TIA/LA), a 4-channel photodiode (PIN) array. The optical signal in the optical fiber is coupled through an optical lens to the receiving photodiode (PIN), where it is converted into a photocurrent. The photocurrent signal is amplified by the TIA/LA amplifier, and then sent to the CDR circuit for retiming, and finally transmitted to the host in the form of high-speed differential signal. The microcontroller reads the signal strength (modulation amplitude) received by the photodiode and reports a loss of the received signal if it is below a set threshold.

Both the transmitter and receiver have the squelch function. When the transmitter side has a signal input, the oscilloscope shows the waveform of the output optical signal as an eye diagram shape, and when there is no signal input, the oscilloscope shows the waveform of the output optical signal as a straight line. When the receiver side has a signal input, the oscilloscope shows the waveform of the output electrical signal as an eye diagram shape, and when there is no signal input, the oscilloscope shows the waveform of the output electrical signal as a straight line.

SFP Block Diagram of Transceiver



SFP Functions Description

AOC-QSFP-4SFP-100G-aaa.aaM-D1D1C SFP module is manufactured using COB (Chip on Board) technology and consists of a microcontroller, a transmitter side optical engine and a receiver side optical engine. The module has built-in clock and data recovery functions, and the working rate range of the transmitter and receiver of the built-in CDR is 25.2-28.1 Gbps. If you need another version of the rate range, you can contact us for special customization.

The microcontroller communicates with the host via a 2-wire serial communication interface and provides module control, status reporting, and monitoring (DOM) functions in accordance with the SFF-8472 standard.

The transmitter side optical engine consists of a clock data recovery circuit (CDR), a laser driver circuit (LD), a VCSEL laser, and a monitoring photodiode (MPD). The high-speed differential electrical signals output from the host is restored and shaped by the CDR. The restored electrical

signal send to the laser driver and drive the VCSEL lasers to generate optical signals. The optical signals are coupled into the optical fiber through an optical lens. The optical engine integrates a monitoring photodiode for output optical power detection.

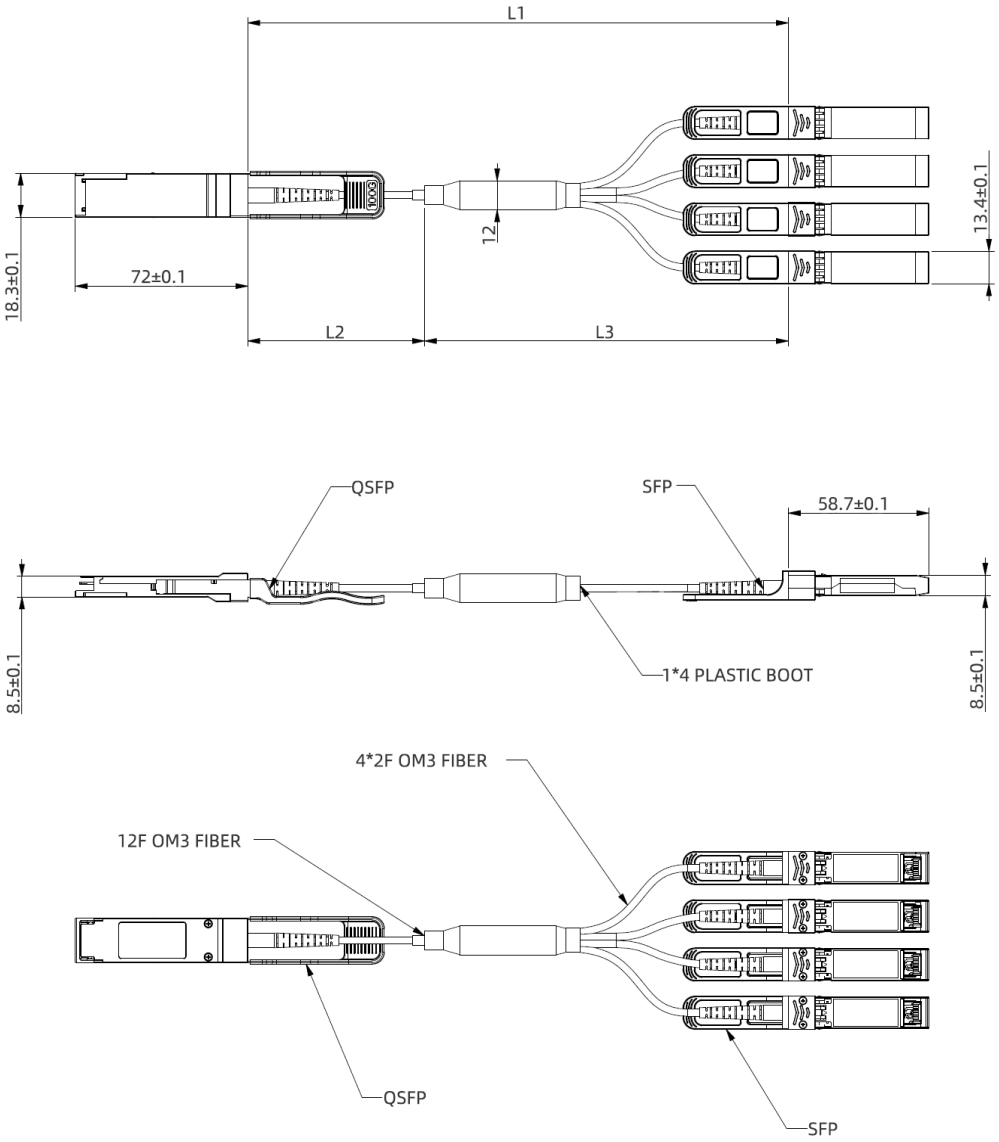
The receiver side optical engine consists of a photodiode (PIN), a signal amplifier (TIA/LA) and a receiver clock data recovery circuit (CDR). The optical signal in the optical fiber is coupled through an optical lens to the receiving photodiode (PIN), where it is converted into a photocurrent. The photocurrent signal is amplified by the TIA/LA amplifier, and then sent to the CDR circuit for retiming, and finally transmitted to the host in the form of highspeed differential signal. The microcontroller reads the signal strength (modulation amplitude) received by the photodiode and reports a loss of the received signal if it is below a set threshold.

Both the transmitter and receiver have the squelch function. When the transmitter side has a signal input, the oscilloscope shows the waveform of the output optical signal as an eye diagram shape, and when there is no signal input, the oscilloscope shows the waveform of the output optical signal as a straight line. When the receiver side has a signal input, the oscilloscope shows the waveform of the output electrical signal as an eye diagram shape, and when there is no signal input, the oscilloscope shows the waveform of the output electrical signal as a straight line.

Optical Cable Details

Parameter	Min	Typ	Max	Unit	Remarks
Jacket Material		LSZH			
Jacket Color		Aqua Green			Other colors available on request
Flammability Rating		OFN			Other ratings available on request
Outer Diameter	2.8	3.0	3.2	mm	
Tensile Load (Short Term)			200	N	
Tensile Load (Long Term)			100	N	
Crush Resistance	10			N/mm	IEC 60794-1-21
Impact Resistance	0.5			N•m	IEC 60794-1-21
Flexing	300			Cycles	IEC 60794-1-21
Twist Bend					IEC 60794-1-21
Cable to SFP+/QSFP+ Plug Connection			90	N	
Bend Radius (Short Term)	25			mm	
Bend Radius (Long Term)	30			mm	

Dimensions

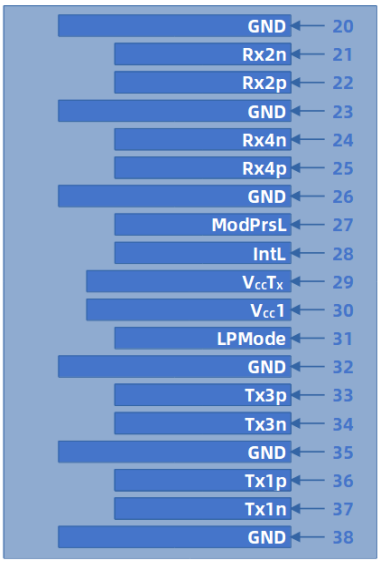


ALL DIMENSIONS ARE ±0.2 mm UNLESS OTHERWISE SPECIFIED
UNIT: mm

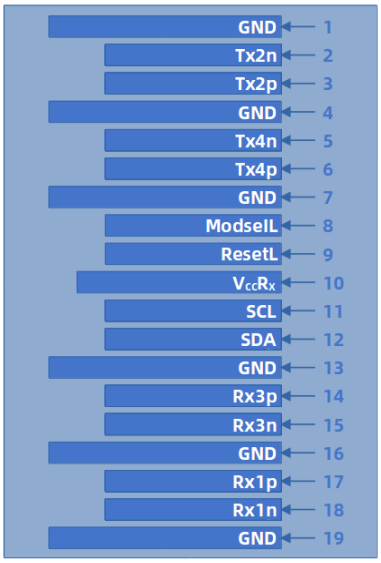
Length (L1)	Length (L2)	Length (L3)
1 M	0.33 M	0.67 M
2 M	0.67 M	1.33 M
3 M	1 M	2 M
≥5 M	L1-L3	3 M

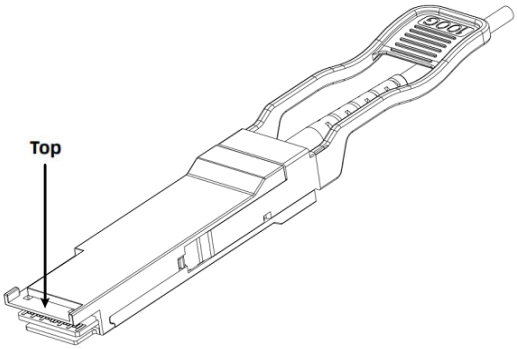
QSFP Electrical Pad Layout

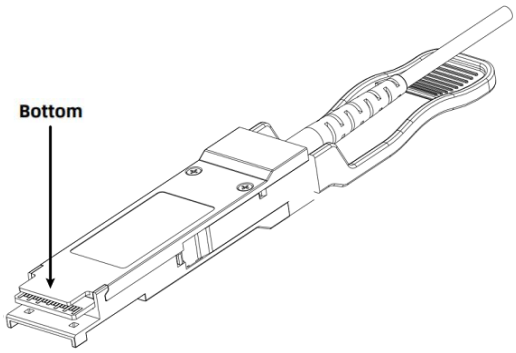
Top View of Board



Bottom View of Board

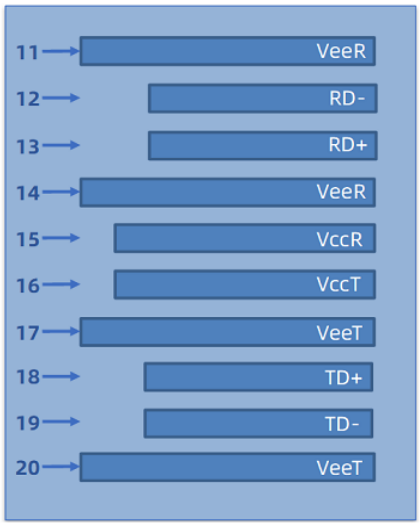




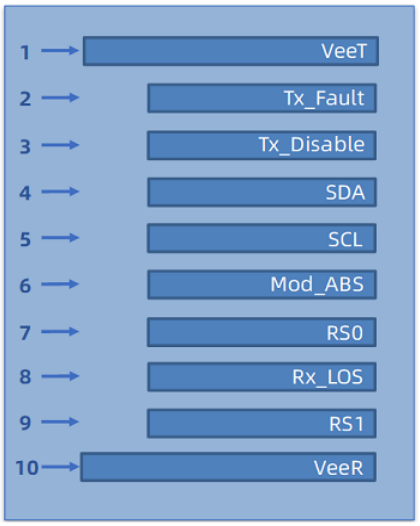


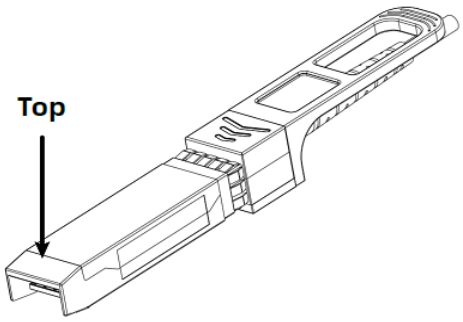
SFP Electrical Pad Layout

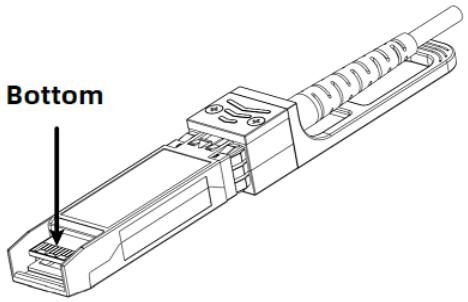
Top View of Board



Bottom View of Board







QSFP Pin Assignment

PIN #	Symbol	Description	Remarks
1	GND	Ground	5
2	Tx2n	Transmitter Inverted Data Input, Lane2	
3	Tx2p	Transmitter Non-Inverted Data Input, Lane2	
4	GND	Ground	5
5	Tx4n	Transmitter Inverted Data Input, Lane4	
6	Tx4p	Transmitter Non-Inverted Data Input, Lane4	
7	GND	Ground	5
8	ModSelL	Module select pin, the module responds to two-wire serial communication when low level	1
9	ResetL	Module Reset	2
10	$V_{cc}R_X$	+3.3 V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	5
14	Rx3p	Receiver Non-Inverted Data Output, Lane3	
15	Rx3n	Receiver Inverted Data Output, Lane3	
16	GND	Ground	5
17	Rx1p	Receiver Non-Inverted Data Output, Lane1	
18	Rx1n	Receiver Inverted Data Output, Lane1	
19	GND	Ground	5
20	GND	Ground	5
21	Rx2n	Receiver Inverted Data Output, Lane2	
22	Rx2p	Receiver Non-Inverted Data Output, Lane2	
23	GND	Ground	5
24	Rx4n	Receiver Inverted Data Output, Lane4	
25	Rx4p	Receiver Non-Inverted Data Output, Lane4	
26	GND	Ground	5
27	ModPrsL	Module insertion indication pin, grounded inside the module	
28	IntL	Interrupt	4
29	$V_{cc}T_X$	+3.3 V Power Supply transmitter	
30	$V_{cc}1$	+3.3 V Power Supply	
31	LPMode	Low power mode, pull-up to Vcc inside the module	3
32	GND	Ground	5

33	Tx3p	Transmitter Non-Inverted Data Input, Lane3	
34	Tx3n	Transmitter Inverted Data Input, Lane3	
35	GND	Ground	5
36	Tx1p	Transmitter Non-Inverted Data Input, Lane1	
37	Tx1n	Transmitter Inverted Data Input, Lane1	
38	GND	Ground	5

Notes:
1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL is High, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module
2. The module restart pin, when the low level on the ResetL pin lasts longer than the minimum pulse length, resets the module and restores all user modules to their default state. When performing reset device, the host should ignore all status bits. Until the module reset interrupt is completed, please note that during hot plugging, the module will issue this information to complete the reset interrupt without resetting
3. When the pin is high, it means that the module is running in low power mode and the transmitter will be turned off; when the pin is low, it means that the module is running in non-low power mode and the module works normally
4. IntL is the output pin, which is the open collector output and must be pulled up to Vcc on the motherboard. When it is low, it indicates that the module may malfunction. The host uses a 2-wire serial interface to read internal status
5. Circuit ground is internally isolated from chassis ground

Pin Assignment

PIN #	Symbol	Description	Remarks
1	VeeT	Transmitter ground (common with receiver ground)	1
2	Tx_Fault	Transmitter fault	
3	Tx_Disable	Transmitter disable. Laser output disabled on high or open	2
4	SDA	2-wire serial interface data line	3
5	SCL	2-wire serial interface clock line	3
6	Mod_ABS	Module absent. Grounded within the module	3
7	RS0	No connection required	
8	Rx_LOS	Loss of signal indication. Logic 0 indicates normal operation	4
9	RS1	No connection required	
10	VeeR	Receiver ground (common with transmitter ground)	1
11	VeeR	Receiver ground (common with transmitter ground)	1
12	RD-	Receiver Inverted DATA out. AC coupled	
13	RD+	Receiver Non-inverted DATA out. AC coupled	
14	VeeR	Receiver ground (common with transmitter ground)	1
15	VccR	Receiver power supply	
16	VccT	Transmitter power supply	
17	VeeT	Transmitter ground (common with receiver ground)	1
18	TD+	Transmitter Non-Inverted DATA in. AC coupled	
19	TD-	Transmitter Inverted DATA in. AC coupled	
20	VeeT	Transmitter ground (common with receiver ground)	1

Notes:
1. Circuit ground is internally isolated from case
2. Disabled: $T_{DIS}>2$ V or open, Enabled: $T_{DIS}<0.8$ V
3. Should be pulled up on the host board with a 4.7 kΩ to 10 kΩ resistor to a voltage between 2 V and 3.6 V
4. LOS is open collector output

References

1. IEEE standard 802.3

2. SFF-8402 Specification for SFP+ 1X 28 Gb/s Pluggable Transceiver Solution (SFP28)

3. SFF-8472 Specification for Management Interface for SFP+

4. SFF-8636 Specification for Management Interface for 4-lane Modules and Cables